University of Alberta

A Digital Predictive Current Controller for Single-Phase PWM Rectifier

By

Jin Fang

A thesis submitted to the faculty of graduate studies and research in partial fulfillment of the requirement of the degree of **Master of Science**.

Department of Electrical and Computer Engineering

Edmonton, Alberta

Fall, 2004

Library and Archives Canada

Published Heritage Branch

395 Wellington Street
Ottawa ON K1A 0N4
Canada

Bibliothèque et Archives Canada

Direction du Patrimoine de l'édition

395, rue Wellington
Ottawa ON K1A 0N4
Canada

Your file Votre référence
ISBN: 0-612-95742-X
Our file Notre référence
ISBN: 0-612-95742-X

The author has granted a non-exclusive license allowing the Library and Archives Canada to reproduce, loan, distribute or sell copies of this thesis in microform, paper or electronic formats.

The author retains ownership of the copyright in this thesis. Neither the thesis nor substantial extracts from it may be printed or otherwise reproduced without the author's permission.

L'auteur a accordé une licence non exclusive permettant à la Bibliothèque et Archives Canada de reproduire, prêter, distribuer ou vendre des copies de cette thèse sous la forme de microfiche/film, de reproduction sur papier ou sur format électronique.

L'auteur conserve la propriété du droit d'auteur qui protège cette thèse. Ni la thèse ni des extraits substantiels de celle-ci ne doivent être imprimés ou aturement reproduits sans son autorisation.

In compliance with the Canadian Privacy Act some supporting forms may have been removed from this thesis.

While these forms may be included in the document page count, their removal does not represent any loss of content from the thesis.

Conformément à la loi canadienne sur la protection de la vie privée, quelques formulaires secondaires ont été enlevés de cette thèse.

Bien que ces formulaires aient inclus dans la pagination, il n'y aura aucun contenu manquant.

Canada

Acknowledgements

I am greatly indebted to a multitude of individuals for helping me complete this thesis. First and foremost, I am most grateful for the enthusiastic supervision of Dr. John Salmon. I consider myself fortunate to be his student and working under his guidance. Without him, my graduate studies would not have been so enjoyable and intellectually rewarding. I can only wish Dr. Salmon all the best for the future.

I also appreciate Dr. Xiaoming Zha for his support and help at the beginning of my masters degree. I thank him for sharing his intelligence of the basic concepts and practical knowledge of power electronics. I was deeply impressed by his patience, kindness, and passion.

I would like to thank all members of my thesis defense committee, Dr. Venkata Dinavahi, Dr. C. Robert Koch, for pre-examining this thesis and providing valuable comments and suggestions. Special thanks are due to Dr. Dinavahi for his support and advice during my master studies. I want to thank all the staff at the Power Laboratory for creating a pleasant working environment.

I am grateful to my mother, Zhiqin, and my brother, Siyuan, for their moral support and understanding. They are very dear to me and always in my thoughts.

Last but not least, I want to express my gratitude to my husband Qinghong, for his support and help during this work. His encouragement and patience have ensured the success of my research. Without his support I would not have been able to complete my thesis.

This research was supported by Dr. John Salmon, the department through teaching assistantships, and the government of the province of Alberta.

Table of Contents

Chapter 1 Introduction 1

1.1 Background 2

1.2 Single-Phase Rectifiers with Diodes or Thyristors 3

1.3 Single-Phase PWM Rectifier Topology 4

1.4 Current Control Techniques for PWM Rectifier 9

1.5 Contributions of This Thesis 12

1.6 Organization of This Thesis 12

Chapter 2 Current Control Techniques 14

2.1 Background 14

2.2 Fixed Switching Frequency Current Control 16

2.2.1 Proportional Control 17

2.2.2 Proportional-Integral Control 20

2.2.3 Average Current Mode Control 22

2.2.4 Predictive Current Control 24

2.2.5 Other Reviewed Fixed Switching Frequency Current Control 25

2.3 Hysteresis Current Control 26

2.3.1 Fixed Band Hysteresis Current Control 26

2.3.2 Sinusoidal Band Hysteresis Current Control 29

2.3.3 Delta Modulation Control 31

2.3.4 Variable Band Hysteresis Current Control 33

2.3.5 Zero Average Current Error Control 36

2.4 Summary 38

Chapter 3 Model-Based Predictive Current Control 40

3.1 General Description 40

3.2 Formula Derivation 43

3.2.1 Basic Formulas 44
3.2.2 Expressions of the Supply Current 44
3.2.3 Concepts and Formulas of the Current Error 46
3.3 MATLAB Program Description 48
3.4 Simulated Characteristics 49
3.4.1 Simulation Under the Nominal Condition 49
3.4.2 Simulation Under the Emulated Practical Condition 51
3.5 Summary 56
Chapter 4 Slope Detective Current Control **57**
4.1 General Description 57
4.2 Formula Derivation 61
4.2.1 Two Approaches to Describe the Slopes of the Current Error Signal 62
4.2.2 Prediction on the Slope ---the First Ramping Process 64
4.2.3 Prediction on the Slope ---the Second Ramping Process 70
4.2.4 Determination for the Desired Switching Instant 72
4.3 MATLAB Program Description 74
4.4 Simulated Characteristics 75
4.4.1 Simulation Under the Nominal Condition 75
4.4.2 Effect of the Circuit Parameter Variations 79
4.4.3 Effect of the dc Link Second Harmonic Voltage 80
4.4.4 Effect of the Random Noise 82
4.4.5 Effect of the ac Harmonic Voltages 83
4.5.6 Transient Response 88
4.5.7 Switching Frequency Band 89
4.5 Comparison with Other Current Control Schemes 90
4.5.1 Comparison with Ramp Comparison Control Scheme 90
4.5.2 Comparison with Fix Band Hysteresis Control Scheme 92

4.5.3 Comparison with Variable Band Hysteresis Control Scheme 95
4.6 Summary 101
Chapter 5 Conclusions 102
5.1 Review Main Work 102
5.2 Future Work 104
Bibliography 106
Appendix A Program of Model-Based Predictive Current Control Scheme 110
Appendix B Program of Slope Detective Current Control Scheme 113
Appendix C Program of Ramp Comparison Current Control Scheme 117
Appendix D Program of Fixed Band Hysteresis Current Control Scheme 119
Appendix E Program of Variable Band Hysteresis Current Control Scheme 122
Appendix F Relevant Mathematic Formulas 125

List of Tables

Table 3.1	Circuit parameters of simulation waveforms in Fig. 3.5	50
Table 3.2	Different circuit parameters of simulation waveforms in Fig. 3.7	52
Table 3.3	Different circuit parameters of simulation waveforms in Fig. 3.8	53
Table 3.4	Different circuit parameters of simulation waveforms in Fig. 3.9	54
Table 3.5	Circuit parameters of simulation waveforms in Fig. 3.10	55
Table 4.1	Circuit parameters of the simulation waveforms in Fig. 4.5	76
Table 4.2	Circuit parameters of the simulated waveforms in Fig. 4.6	78
Table 4.3	Different circuit parameters of the simulated waveforms in Fig. 4.8	79
Table 4.4	Different circuit parameters of the simulated waveforms in Fig. 4.9	81
Table 4.5	Different circuit parameters of the simulated waveforms in Fig. 4.10	83
Table 4.6	Different circuit parameters of the simulated waveforms in Fig. 4.11	85
Table 4.7	Different circuit parameters of the simulated waveforms in Fig. 4.13	85
Table 4.8	Different circuit parameters of the simulated waveforms in Fig. 4.15	88
Table 4.9	Circuit parameters of the simulated waveforms in Fig. 4.17	88
Table 4.10	Circuit parameters of the simulation waveforms in Fig. 4.19	92
Table 4.11	Circuit parameters of the simulation waveforms in Fig. 4.21	94
Table 4.12	Circuit parameters of the simulation waveforms in Fig. 4.23	95
Table 4.13	Different circuit parameters of the simulated waveforms in Fig. 4.25	98
Table 4.14	Different circuit parameters of the simulated waveforms in Fig. 4.26	99

List of Figures

Figure 1.1	Single-phase full-wave voltage source PWM rectifier bridge topology	5
Figure 1.2	Simplified model of the single-phase full-wave voltage source PWM rectifier bridge	6
Figure 1.3	Bipolar PWM voltage switching in a line cycle	7
Figure 1.4	Unipolar PWM voltage switching in positive half line cycle	8
Figure 1.5	Unipolar PWM voltage switching in negative half line cycle	8
Figure 1.6	Unipolar PWM voltage switching in a line cycle	8
Figure 1.7	Ramp comparison current control	10
Figure 1.8	Fixed band hysteresis current control	10
Figure 2.1	Inductor current signal and modulated voltage pulse signal	15
Figure 2.2	Block diagram of proportional control	17
Figure 2.3	Triangular carrier and analogue control signal in one switching cycle	18
Figure 2.4	Current error signal *ierr*, supply voltage V_s, and pulse voltage V_i	19
Figure 2. 5	Block diagram of proportional-integral control	21
Figure 2. 6	Average current mode control circuit topology	23
Figure 2.7	Average current mode control waveform	23
Figure 2.8	Block diagram of fixed band hysteresis control	27
Figure 2.9	Fixed band hysteresis current control waveforms	27
Figure 2.10	Block diagram of sinusoidal band hysteresis control	30
Figure 2.11	Sinusoidal band hysteresis current control waveforms	30
Figure 2.12	Block diagram of mixed band hysteresis control	31
Figure 2.13	Block diagram of delta modulation control	31
Figure 2.14	Block diagram of improved delta modulation control	32
Figure 2.15	Variable band hysteresis current control waveforms	34

Figure 2.16	Principle of variable band hysteresis control	34
Figure 2.17	Current error signal under ZACE control	36
Figure 2.18	Block diagram of slope generated hysteresis control	36
Figure 2.19	Principle of ramptime control	37
Figure 3.1	Block diagram of model-based predictive current control	41
Figure 3.2	Current error waveform under model-based predictive control	42
Figure 3.3	Supply current waveform in one PWM switching cycle	45
Figure 3.4	Determination of switching instants by MATLAB program	48
Figure 3.5	Simulated waveforms under the nominal condition	50
Figure 3.6	Simulated waveforms with higher switching frequency	51
Figure 3.7	Simulated waveforms with +20% supply inductance mismatch	52
Figure 3.8	Waveforms with the injected 5% second harmonic in dc link voltage	53
Figure 3.9	Waveforms with random noise in supply voltage	54
Figure 3.10	Waveforms with 5% second harmonic, 3% random noise, 20% inductance mismatch	55
Figure 4.1	Block diagram of slope detective current control scheme	58
Figure 4.2	Principle of slope detective current control	59
Figure 4.3	Current error waveform with fixed frequency clock	62
Figure 4.4	Current error, supply voltage and dc link voltage waveforms	69
Figure 4.5	Simulated waveforms under the nominal condition	76
Figure 4.6	Simulated waveforms with higher switching frequency	77
Figure 4.7	Harmonic spectrum of the supply current in Fig. 4.6 (a) using fundamental of 60Hz	78
Figure 4.8	Simulated waveforms with the different supply inductances	80
Figure 4.9	Waveforms with the injected 5% second harmonic in dc link voltage	81
Figure 4.10	Waveforms with 3% random noise in supply voltage	82
Figure 4.11	Waveforms with 3% ac eleventh harmonic voltage	84

Figure 4.12	Harmonic spectrum of the supply current in Fig. 4.11 (c) using fundamental of 60Hz	85
Figure 4.13	Waveforms with 5% ac 3rd harmonic voltage	86
Figure 4.14	Harmonic spectrum of the supply current with 5% 3rd harmonic in the ac supply voltage	86
Figure 4.15	Waveforms with 5% ac 2nd harmonic voltage	87
Figure 4.16	Harmonic spectrum of the supply current with 5% 2nd harmonic in the ac supply voltage	87
Figure 4.17	Transient response waveforms for the current reference change	89
Figure 4.18	Extremely narrow switching band	90
Figure 4.19	Waveforms of ramp comparison control scheme	91
Figure 4.20	Harmonic spectrum of the supply current in Fig. 4.19 (a) using fundamental of 60Hz	92
Figure 4.21	Waveforms of fixed band hysteresis control scheme	93
Figure 4.22	Harmonic spectrum of the supply current in Fig. 4.21 (a) using fundamental of 60Hz	94
Figure 4.23	Waveforms of variable band hysteresis control scheme	96
Figure 4.24	Harmonic spectrum of the supply current in Fig. 4.23 (a) using fundamental of 60Hz	97
Figure 4.25	Waveforms for both schemes with the maximum 3% random noise of the ac voltage	98
Figure 4.26	Waveforms for both schemes with 5% 2nd harmonic of dc link voltage	98
Figure 4.27	Switching frequency band waveforms for both schemes	99
Figure 4.28	Transient response waveforms for the current reference change	100

List of Abbreviations

ACMC	Average Current Mode Control
ADC	Analogue Digital Conversion
DAC	Digital Analogue Conversion
DM	Delta Modulation
DSP	Digital Signal Processing
GTO	Gate Turn-Off
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Mental-Oxide-Semiconductor Field Effect Transistor
MRA	Model Reference Adaptive
P	Proportional
PI	Proportional Integral
PF	Power Factor
PWM	Pulse-Width-Modulated
RMS	Root Mean Square
SCR	Silicon-Controlled Rectifier
SGH	Slope Generated Hysteresis
TC	Triangular Carrier
THD	Total Harmonic Distortion
ZACE	Zero Average Current Error

Chapter 1 Introduction

Due to the growing usage of nonlinear loads over the last two decades, harmonic contamination in power systems has become an important issue. Two types of rectifiers, the diode rectifier and the thyristor rectifier, are basic and common approaches to convert the power flow from the ac to the dc side. The power diode rectifier is simple and inexpensive, but lacks control on its dc link output voltage. The thyristor rectifier has the feature of allowing control of its output dc link voltage, but suffers from severe performance degradation of its input power quality in comparison with the diode rectifier. A clean and economically feasible solution for power conversion is more desirable than ever before under the request of the global concern of environment pollutions and the evolution of semiconductor technologies.

The Pulse-Width-Modulated rectifier bridge, namely the PWM rectifier in short, is composed of power diodes and power semiconductor switches. Two basic PWM voltage waveforms describe the main operational modes of PWM rectifiers, unipolar PWM voltage switching and bipolar PWM voltage switching. The nature of these PWM waveforms are described in this chapter to provide an introduction to the PWM control techniques examined in this thesis. The inclusion of power semiconductor switches in the PWM rectifier bridge provides full control over both the dc link voltage and the ac supply current. Consequently, the PWM rectifier can be implemented with suitable current control techniques that provide a resistor-like interface between the rectifier and the power utility.

Many research investigations have been undertaken on suitable current control schemes for PWM rectifiers; typical ones are ramp comparison current control [1-4,19], predictive current control [9-14], fixed band hysteresis current control [1-3,19,20] and variable band hysteresis current control [23-26]. Theses current control schemes are discussed in detail as background knowledge of current control techniques.

The basic concept of the ac to dc power conversion is introduced first in this chapter. Two common methods to convert the power flow from the ac to the dc side, diode and thyristor

rectifiers, are described. The circuit topology of single-phase PWM rectifier associated with a corresponding simplified functional model is illustrated. Several typical current control techniques are briefly described. Merits of the proposed control scheme are discussed. The contributions and organization of the thesis are also presented in this chapter.

1.1 Background

The widespread application of power electronics [34] reveals that about 60% of the electric energy consumed in North America in recent years is processed by power electronic systems. From consumer electronics to high power industrial variable speed drives, and even in more exotic areas such as space programs, power electronic technology provides many benefits to our society. There are several factors attributed to the growth of power electronics over the years, one of significant factor is the advent of more advanced power semiconductor components and associated control electronics.

The evolution of power electronics technology dates back from the first appearance of mercury arc rectifier as "static" power conversion in the early years of 20th century. However, the performance of this rectifier is now considered poor by today's standards in many practical industrial applications. The discovery of semiconductor led to the inventions of power diodes, thyristors, and ultimately other advanced power transistors, such as the IGBT, power MOSFET, GTO, etc. Advances in power semiconductor fabrication technologies have brought improvements in the characteristics of power semiconductor with higher voltage and current ratings, faster switching speeds, improved reliability and more feasible prices for practical industrial applications. In general, power electronic technology concerns the control of raw electrical power to meet the requirements of various loads such as motors and electrical/electronic devices.

Due to the different characteristics of drawing power from the utility and delivering power to a load, power electronic converters may be considered as an electrical power interface, or buffer, between the utility and the load. Power conversion from the electrical utility is the

principle application discussed in this thesis, focusing mainly on applications using the single-phase rectifier to control the power flow from the ac utility to a capacitor smoothed dc link. The switching converters, namely forced-commutated converters, often referred to as Pulse-Width-Modulated (PWM) controlled rectifiers, are fully controllable. The naturally commutated converters, namely line-frequency converters, often referred to as SCR rectifiers or diode rectifiers, are the counterparts of the forced-commutated converters and are introduced as background knowledge.

1.2 Single-Phase Rectifiers with Diodes or Thyristors

The simple and inexpensive line-frequency diode rectifier [2,3] is widely used as a direct interface between the utility ac voltage source and the dc voltage output. The diode rectifier is an uncontrolled rectifier because the diodes switch on and off at the line frequency and are phase locked to the line-voltage waveform. In most applications, a large dc link filter capacitor is desirable to lower the natural ripple in the dc link output. However, the desired ripple free dc link voltage performance, inevitably introduces discontinuous dc and ac currents to the converter circuit. This discontinuous ac current of the diode rectifier contains a large amount of harmonics and deteriorates the performance of the circuit as seen from the power system. In addition, the high current peaks associated with these currents, increase the volt-ampere ratings of the power electronic devices and utility equipment, such as transformers, transmission lines, and generators, provide more electrical stress on the power semiconductor, and distort the waveshape of the supply voltage, hence introduces interference with other loads.

The thyristor rectifier [2,3] is a line-frequency phase-controlled rectifier that produces a controllable dc link voltage by varying the firing angle based on the requirements of the application. Although the switches in the thyristor rectifier switch at the supply frequency, just as the diode rectifier, the devices can be used to control the dc output voltage by controlling the phase position in the ac cycle associated with the on and off periods of the devices. However, this "phase-control" of the thyristor devices, based upon the magnitude of the dc output,

introduces not only a larger amount of harmonics, but also a reactive power component. In other words, the voltage control feature of the thyristor rectifier, in comparison with the diode rectifier, brings a poorer performance of the rectifier as viewed from the power utility.

The increased use and wider application of utility rectifiers have presented a significant negative impact on the power system, essentially due to the injection of a large amount of low frequency current harmonics into the utility supply grid. The negative effects of these low order harmonics include: a reduction in power factor, unnecessary extra heating and losses, and decreasing power equipment lifespan, etc [2,3]. Thus much effort and many investigations have been conducted to lower cost, to increase reliability, and to improve the effectiveness of the rectifier for power conversion [32,34]. One approach to minimize the impact is to filter the low order harmonics produced by the rectifier with either passive harmonic filters or active power filters [2]. However, these filter schemes are not capable of eliminating the low order harmonics from being generated in the first place and often introduce other problems such as parasitic oscillations with the utility and other loads [2,3]

1.3 Single-Phase PWM Rectifier Topology

The single-phase PWM rectifier topology, see Fig. 1.1, is basically the single-phase switch-mode inverter topology with an operation mode as a rectifier, which converts the power flow from the ac to the dc side. There are a number of rectifier topologies based on different application requirements, such as the voltage source rectifier topology or the current source rectifier topology, single-phase rectifier topology or three-phase rectifier topology, half-bridge topology or full-bridge topology [2]. The work presented in this thesis concerns the single-phase full-wave voltage source PWM rectifier topology, as shown Fig. 1.1. Each functional switching element of the rectifier bridge consists of a switchable power transistor, such as IGBT, GTO or power MOSFET [2], and a freewheeling power diode connected in parallel. The body of a rectifier as a single-phase full-wave bridge in this case is composed of four such switching elements.

This rectifier bridge is used as an interface between the utility source and the load. The power transistor has the capability of being fully controlled to turn on or off whenever required and at a frequency much higher than the supply frequency. Due to this nature, the rectifier is also referred to as a "forced-commutated rectifier". This control feature of the rectifier bridge allows it to be controlled on both its capacitor smoothed dc link output voltage and its ac supply input current waveshape using Pulse-Width-Modulated switching patterns.

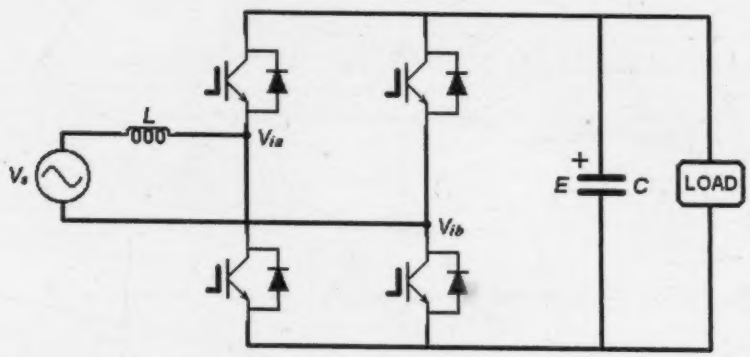


Figure 1.1 Single-phase full-wave voltage source PWM rectifier bridge topology

The basic control of a voltage source rectifier uses a pre-established sinusoidal current template as a reference to waveshape the supply current. Based upon this current template and the dc link voltage required by the load operation, numerous PWM controllers can be used to control the rectifier switching pattern depending upon the terms of the different control strategies. A common issue for many of these controllers is not only to regulate the dc link voltage as required, but also to control accurately the ac line current waveshape to minimize the harmonic contamination to the utility source. In other words, the PWM rectifier could have its dc link voltage fully controlled while shaping the ac line current to reach or at least close to a unity power factor operational performance. Unity power factor operation represents the ideal performance.

Although this topology produces a lower harmonic pollution and better power factor performance, it also has its own disadvantages. The complexity of the control schemes and the

economic feasibility of the switching elements are two other considerations amongst many when considering the application. In addition, the side effect of the fast switching capability introduces the electromagnetic interference pollution. Nevertheless, the increasing global concerns about the effects of environmental pollutions lead to a strict enforcement of harmonic standards. On the other hand, advances in semiconductor fabrication and the integration of technologies, show a way of bringing forward more cost-effective power semiconductor. Many researches and investigations are focused on the control schemes on the PWM rectifier. The details are discussed in Chapter 2.

A point worth noting here is that the dc link output voltage of a PWM controlled rectifier has to be kept higher than the voltage of a simple diode rectifier bridge. Otherwise, the four diodes shown in Fig. 1.1 can conduct, leading to the PWM rectifier to behave like a common diode rectifier bridge and thus losing its feature of being switched and controlled. A simplified model of the single-phase full-wave voltage source PWM rectifier bridge, used for analysis and simulation purpose in this thesis, is illustrated in figure 1.2.

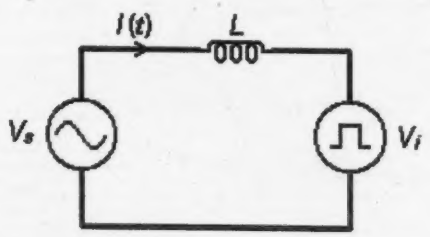


Figure 1.2 Simplified model of the single-phase full-wave voltage source PWM rectifier bridge

Generally, the resistance of the inductor is considered relatively small and less functional with respect to the inductance. The resistance component is considered negligible during the analysis and simulation procedures. Based on the ordinary operation condition of the PWM rectifier, an assumption of a relative stable dc link output voltage is also considered to be a reasonable situation. To simplify the relevant formulas, a constant dc link voltage E is assumed and employed during the analysis procedures. However, the natural ripple, mainly the second

harmonic of the dc link output voltage, can be relatively significant hence cannot be ignored during the simulation process.

The ac voltage source V_s represents the power source, as shown in figure 1.2. The voltage source V_i in the model represents the PWM voltage signal at the input terminals to the rectifier bridge. The current through this loop is actually the ac supply current, whose control of its waveshape is the main concern of the work presented in this thesis.

There are two basic PWM operational modes for the simple four-switch PWM rectifier bridge: *bipolar PWM voltage switching* scheme and *unipolar PWM voltage switching* scheme. In bipolar PWM, the pulse voltage source V_i switches between $-E/2$ and $+E/2$ voltage levels during a line cycle, as shown in Fig. 1.3, resulting in high switching voltage stresses on the electronic components and loads.

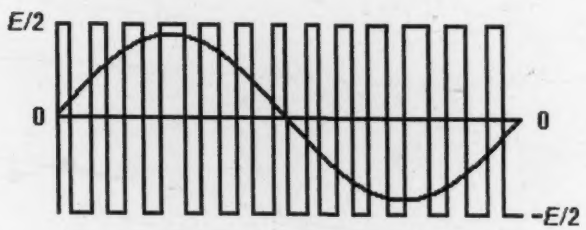


Figure 1.3 Bipolar PWM voltage switching in a line cycle

$$V_i = \begin{cases} E; \\ -E; \end{cases} \tag{1.1}$$

As opposed to bipolar PWM voltage waveform, in unipolar PWM the output of the pulse voltage source V_i jumps between zero and $+E$ during the positive half cycle of the ac voltage signal, as shown in Fig. 1.4, or between zero and $-E$ during the negative half cycle of the ac voltage signal, as shown in Fig. 1.5. Compared with bipolar PWM , unipolar PWM in Fig. 1.6 generates lower harmonics than those of bipolar switching scheme. This is because it effectively doubles the harmonic frequency of the PWM voltage waveform that pushes the harmonics to higher values. Due to these advantages, the work in this thesis is focused mainly on unipolar

PWM.

Figure 1.4 Unipolar PWM voltage switching in positive half line cycle

$$V_i = \begin{cases} 0; \\ E; \end{cases} \tag{1.2}$$

Figure 1.5 Unipolar PWM voltage switching in negative half line cycle

$$V_i = \begin{cases} 0 \\ -E; \end{cases} \tag{1.3}$$

Hence, the two expressions for V_i could be combined for whole ac voltage cycle as follows:

$$V_i = \begin{cases} 0; \\ sign(V_s) \cdot E; \end{cases} \tag{1.4}$$

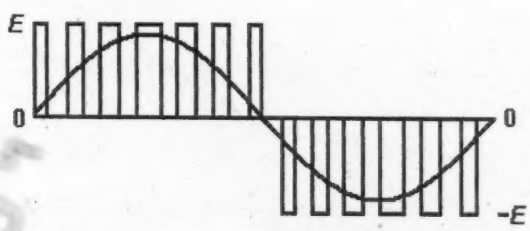


Figure 1.6 Unipolar PWM voltage switching in a line cycle

The sinusoidal voltage source V_s in figure 1.2 represents the utility voltage source and is described by the following equation, in which V_{pk} represents the peak magnitude of the phase voltage, ω designates the line frequency, and t represents time.

$$V_s = V_{pk} \sin \omega t \tag{1.5}$$

A differential equation is derived based on the combined expression of the pulse voltage source V_i and the simplified mode of rectifier bridge depicted in Fig. 1.2. The inductance L is very important in the control process, the voltage impressed across this component is controlled to get an instantaneous balance between the phase voltage source V_s and the modulated voltage source V_i, as shown in Eq. (1.6). The basic equations for unipolar PWM and bipolar PWM operations are shown in Eq. (1.6) and Eq. (1.7) respectively. The detailed derivation and implication of the basic equation shown in Eq. (1.6) is presented in Chapter 3.

$$L\frac{di}{dt} = V_s - V_i = \begin{Bmatrix} V_s \\ V_s - sign(V_s) \cdot E \end{Bmatrix} \tag{1.6}$$

$$L\frac{di}{dt} = V_s - V_i = \begin{Bmatrix} V_s + E/2 \\ V_s - E/2 \end{Bmatrix} \tag{1.7}$$

1.4 Current Control Techniques for PWM Rectifier

The switchable and controllable PWM rectifier has drawn many research interests in recent years. Two basic control schemes, ramp comparison current control [1-3,19] and fixed band hysteresis current control [1-3,19,20], are the foundations of the two significant categories of current control technology based upon analogue techniques.

Ramp comparison current control [1] is a constant switching frequency modulation technique that generates the switching instant by comparing a voltage control signal with a triangular carrier reference, as shown in Fig. 1.7. The constant switching frequency produces more defined high order frequency harmonics that are relatively easy to filter. However, due to the inherent nonlinear characteristics of the rectifier bridge, ramp comparison current control cannot force the current to follow the current template with sufficient accuracy. The low order harmonic distortion of the controlled ac supply current still presents with this control scheme [4,21]. A simple solution for this problem is a higher switching frequency that has with increased switching losses as a side effect.

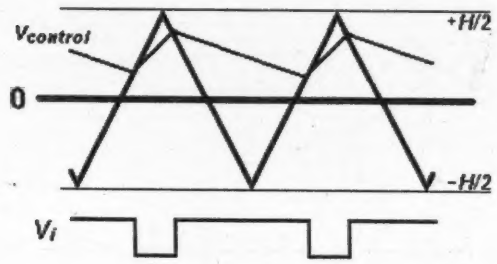


Figure 1.7 Ramp comparison current control

Fixed band hysteresis current control has the merits of being simple and stable regardless of the circuit parameters variations [1,19,20]. This approach attempts to place limits on the variation of the current error signal using a pre-defined current error hysteresis band so that an even current error signal is developed, see Fig. 1.8. Nevertheless, the variation of the switching frequency brings forward severe low order harmonic distortion of the ac supply current. Other negative effects brought along with the variable switching frequency are the extra switching losses and the higher stresses on the switching components. Many research investigations based upon controlling the hysteresis band for the current error signal have been proposed in recent years [23-26].

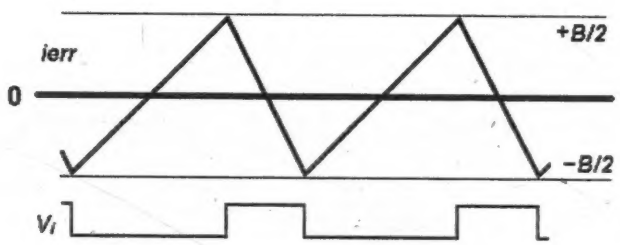


Figure 1.8 Fixed band hysteresis current control

The advances of digital technology bring not only the evolution of the original analogue version of control schemes, but also new concepts that take the full advantage of digital technology. Variable band hysteresis current control [23-26] and predictive current control [9-14] are two categories of many control schemes that are based on digital technology and that

have been the attention of recent research investigations.

Variable band hysteresis current control attempts to maintain the constant switching frequency by regulating the current error signal within a desired variable hysteresis band. For this control scheme, the performance of PWM rectifier operation is much improved with respect to the analogue-based fixed band hysteresis current control scheme. However, the variations of the switching frequency cannot be completely eliminated, and are potentially severe in real applications [25-26].

Predictive current control primarily concentrates on obtaining constant switching frequency, while generating the desired switching instant to minimize the average current error. This control method attempts to predict the intended switching instant based upon an established model of rectifier bridge and is combined with various control laws. Satisfactory bridge performance can be achieved provided the model parameters match the actual circuits parameters. However, this scheme is generally considered as being sensitive to variations in circuit parameters [9-14].

To overcome the above deficiencies, a novel digital-based constant switching frequency unipolar PWM current control scheme, ***slope detective current control***, is proposed in this thesis. As implied by its name, the generation of the intended switching instant is based upon the current error signal slope of the previous two successive switching cycles. This minimizes the low order harmonics during steady state operation without requiring knowledge of the circuit parameters, e.g. the supply voltage and ac side circuit parameters. In addition, accurate control of the ac current can be achieved so that unity power factor is obtained.

The proposed control scheme is stable and independent of changes in circuit parameters, ac supply voltage distortions, or dc link voltage variations. The high order harmonic currents produced by this control are very easy to filter, avoiding the use and cost of an extra low order harmonic filter. It does not require very high switching frequency to obtain satisfactory performance. The combination of low switching losses and high performance make this scheme an attractive alternative compared to other relevant schemes. It is suitable for accurate current

control and high power applications.

The proposed control scheme is based upon digital technology that involves real-time calculations for predictive and accurate control purpose. In addition, the constant switching frequency is ensured by the precise digital clock rate. Time delay is a common issue of digital implementations, due to the DAC or ADC conversion time, the propagation time, and the computational time [7,33]. Two samplings of the ac supply current per cycle are required by this scheme, resulting the reduction in time delay.

1.5 Contributions of This Thesis

The first contribution of this thesis is to examine a specific technique for controlling the input current waveshape to a single-phase PWM rectifier that achieves a unity input power factor, where the current error relative to a demand current template is minimized over a switching cycle. Mathematic equations are used to give theoretical proof of the proposed control algorithm. Simulations emulating real experimental environment are performed to verify the effectiveness of the control scheme.

The second contribution of this thesis is to analyse and compare the simulated characteristics with those of other current control schemes. Merits of the proposed scheme, such as fixed switching frequency, low switching losses, zero-centered current error, unity power factor, low inductor current ripple, independent of changes in circuit parameters, stable and fairly fast transient response, are clarified by the comparison. In addition, a model-based predictive current control is proposed as foundation for a slope detective current control.

1.6 Organization of This Thesis

Background knowledge of current control and PWM rectifier are introduced in Chapter 1. Current control techniques are reviewed in Chapter 2. Detailed descriptions and simulated characteristics of this scheme, from the original model-based predictive control to the enhanced

form, slope detective current control, are presented in Chapter 3 and Chapter 4, respectively. Comparison between this scheme and other current control schemes, such as ramp comparison control, fixed band hysteresis control, and variable band hysteresis control are exhibited in Chapter 4. Conclusion and future work of this thesis are presented in Chapter 5.

Chapter 2 Current Control Techniques

Introducing the power semiconductor switches to the ac to dc power conversion provides two benefits, control over the ac inductor current and the bridge output dc link voltage. Generally, the output voltage and the inductor current are separately controlled by an outer control loop and an inner control loop respectively. This thesis concentrates on the current control techniques associated with the inner current control loop applied on the single-phase ac to dc PWM rectifier topology, shown in Fig. 1.1. Both bipolar PWM control and unipolar PWM control are discussed in this chapter [2,3].

Current control techniques are reviewed and classified into two main groups, fixed switching frequency current control and hysteresis current control. Examples of fixed switching frequency current control schemes include: proportional control; proportional-integral control; average current mode control; predictive current control; model-based constant switching frequency control. Examples of hysteresis current control schemes include: fixed band hysteresis control; sinusoidal band hysteresis control; delta modulation control; variable band hysteresis control; zero average current error control.

2.1 Background

In an attempt to maintain the control over the supply current in one PWM switching cycle, a modulated voltage pulse train is generated. This pulse train must have two possible voltage states, high or low relative to each other. To achieve the desired control goal, one voltage state must always result in the current ramping in one direction, while the other voltage state must always result in the current ramping in the opposite direction [35], as shown in Fig. 2.1. The main control goal can be summarized as being to choose a desired switching instant so that the current follows the intended trajectory.

The pulse width in a pulse train is varied continuously and is controlled to minimize the

low order harmonics in the ac supply current. The accurate tracking of the current along with the desired current reference is associated with benefits such as: low harmonic distortion; high power factor; low voltage-ampere ratings of the power electronic equipment. On the other hand, pulse voltage source produces high order harmonics, centered around the switching frequency or double switching frequency, depending upon which PWM switching scheme is chosen, e.g. bipolar PWM scheme or unipolar PWM scheme. If the switching frequency is high enough, the two groups of harmonics, fundamental and high order harmonics, are widely separated from each other and the latter are easily filtered [32].

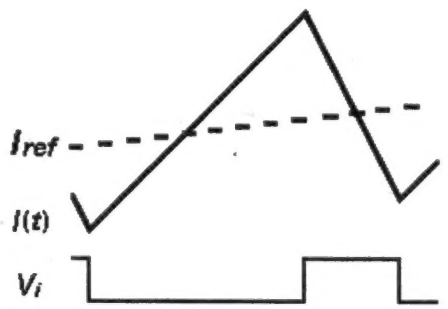


Figure 2.1 Inductor current signal and modulated voltage pulse signal

Pulse width modulation technique also produces continuously varying current ripple oscillating around its reference. The inductor current ripple depends not only on the PWM voltage waveform type, but also on the line voltage V_s, the supply inductance L, the intended switching frequency f or modulation period T, and the dc link voltage E, referring to Eq. (2.9) and Eq. (2.26). In the case of the ac to dc power conversion, the dc link voltage and the other circuit parameters are normally considered relatively constant, but the line voltage V_s varies sinusoidally over a line cycle. This latter feature normally determines that the inductor current ripple and the switching frequency cannot be maintained constant at the same time.

If the switching frequency is defined to be fixed, the inductor current ripple must vary with the supply voltage to maintain the control over the supply current. For the same reason, if the inductor current ripple is regulated to be constant, the switching frequency must vary with the

supply voltage. Due to this, current control schemes are generally categorized into two groups, fixed switching frequency current control and hysteresis current control [32].

Fixed switching frequency current control [1-19] basically keeps the switching frequency constant while allowing the current ripple to vary. Significant performance to judge the control scheme would be harmonic distortions and current ripple variations. Another distinct feature for this type of control scheme is that the average output of PWM cycle can be made to be linearly related to control variables. A linear transfer function can always be found between the voltage control signals and the switching frequency together with the circuit parameters, either estimated or sampled. Due to the fixed switching frequency, the switching losses are relatively low, making it suitable for high power applications.

Hysteresis current control [1-3,19-31] generally concentrates on the regulation about the magnitude of the current ripple. Either fixed band hysteresis [1-3,19,20,28-31] or variable band hysteresis control scheme [23-26] is widely investigated. For the former, it is basically analogue-based, simple and extensively used, while the constant switching frequency is lost. For the latter, it is generally digital-based algorithm to obtain the variable hysteresis band that maintains the constant switching frequency. The determination of the variable hysteresis band is based upon circuit parameters, recent previous hysteresis band, intended switching frequency, or current error zero crossing. Significant performance to evaluate the control algorithm would be the switching band variations and harmonic distortions.

2.2 Fixed Switching Frequency Current Control

Fixed switching frequency current control [1-19] is basically constant switching frequency scheme whose voltage reference signal or the other control signals, such as the inductor current, the inductor voltage, the average inverter output voltage, or the duty cycle, can generally be defined by circuit parameters, control variables, and a intended switching frequency in the form of linear transfer functions. The basic analogue fixed switching frequency control schemes are proportional control, proportional-integral control and average current mode control [1-7,19].

Many digital control schemes have also been developed with the improvements and availability of suitable digital technology [8-10,12-15,17-18]. Predictive control schemes based upon the linear transfer function or the linear circuit model in conjunction with the constant switching frequency are introduced in this section [9-14].

2.2.1 Proportional Control

A proportional current controller [1-4,19], or P controller in short, is shown in a block diagram form in Fig. 2.2. The scheme is also known as ramp comparison control [1], and triangular carrier current control, or TC in short [19]. The current error between the actual current and its reference is amplified or fed through a proportional current controller. To generate the required PWM pattern, the output signal of the current controller $V_{control}$ is compared with the fixed frequency triangular carrier through PWM modulator, as shown in Fig. 1.7. The PWM modulator includes either one or two analogue comparators per phase, depending on whether bipolar PWM scheme or unipolar PWM scheme is employed [2,3].

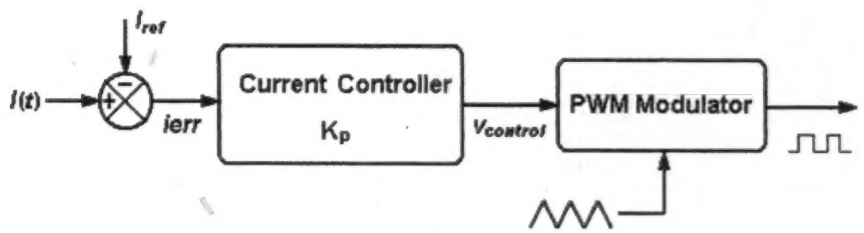


Figure 2.2 Block diagram of proportional control

In addition to the various benefits of analogue-based scheme, this control scheme limits the maximum switching frequency to the constant triangular carrier frequency. As a result, more defined and easier to be filtered harmonics are produced with respect to fixed band hysteresis control, making it more suitable for high power applications. However, this scheme produces both magnitude and phase errors of the inductor current in steady state operation [4,21]. Besides, the voltage control signal being compared with the triangular carrier signal can cause multiple

switching edges. This problem could be avoided either to add some hysteresis band to the analogue comparator or to limit the magnitude of the triangular carrier [4,22], see section 2.2.2. The simulated characteristics of this control scheme are compared with the proposed control scheme in Chapter 4.

The linear transfer function between the average current error signal $ierr_{ave}$ and the average voltage signal V_{ave} is also a simple proportional part for this control scheme. In every PWM switching cycle, the average voltage signal V_{ave} is compared with the triangular carrier, as shown in Fig. 2.3. The switching of the PWM rectifier occurs when the two signals intersect each other. H designates the peak-to-peak magnitude of the triangular carrier waveform, and D represents the duty cycle in a switching period, see Fig. 2.3. Assuming K_p equal to 1, the tracking ability of the supply current of proportional control scheme is derived as follows:

$$V_{ave} = K_p \cdot ierr_{ave} = ierr_{ave} \tag{2.1}$$

For the two analogical triangles in Fig. 2.3, it has:

$$\frac{V_{ave}}{H/2} = \frac{ierr_{ave}}{H/2} = \frac{1/4 - D/2}{1/4} = 1 - 2D \tag{2.2}$$

Rearranging the above equation, gives:

$$ierr_{ave} = H/2 \cdot (1-2D) = H \cdot (1/2 - D) \tag{2.3}$$

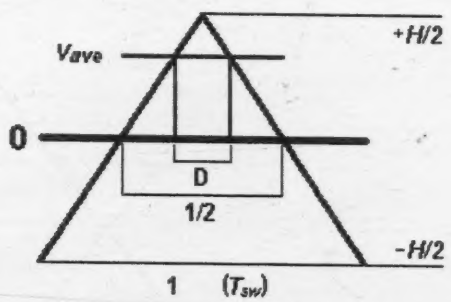


Figure 2.3 Triangular carrier and analogue control signal in one switching cycle

The actual supply current of this scheme experiences distortion whereby the current error

reaches the peak of the supply voltage [4]. This is explained by the above equation. For this control method, the average current error in one PWM switching cycle is equal to zero unless the duty cycle is equal to 1/2. For PWM rectifiers with the ac to dc power conversion purpose, the sinusoidal ac supply voltage source determines that the suitable duty cycle cannot be kept fixed to 1/2 in a line cycle. It varies along with the ac supply voltage, referring to Eq. (2.10) for unipolar PWM scheme and Eq. (2.27) for bipolar PWM scheme.

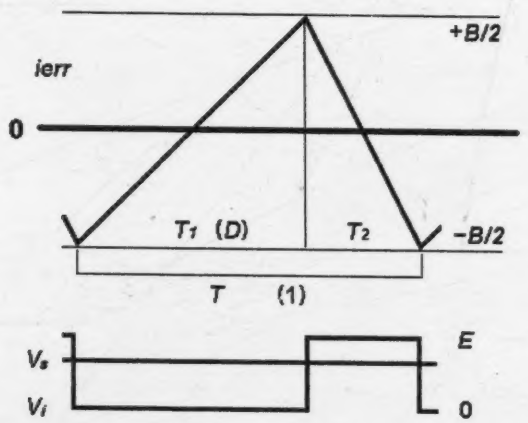


Figure 2.4 Current error signal *ierr*, supply voltage V_s, and pulse voltage V_i

For the single-phase PWM rectifier with unipolar PWM control scheme, assume the supply voltage is invariable in every PWM switching cycle and the supply current error is well regulated within the $+B/2$ to $-B/2$ current band, as shown in Fig. 2.4. According to Eq. (1.6), the switch on-time T_1 is expressed as:

$$L\frac{B/2+B/2}{T_1}=V_s \tag{2.4}$$

Rearranging the above equation yields:

$$T_1=\frac{L\cdot B}{V_s} \tag{2.5}$$

Similarly, for the switch off-time T_2, it has:

$$L\frac{-B/2-B/2}{T_2}=V_s-E \tag{2.6}$$

Rewriting the above equation, gives:

$$T_2=\frac{-L\cdot B}{V_s-E} \tag{2.7}$$

The switching period is the sum of the switch on-time T_1 and the switch off-time T_2,

$$T=T_1+T_2=\frac{L\cdot B}{V_s}+\frac{-L\cdot B}{V_s-E}=\frac{L\cdot B\cdot E}{V_s\cdot(E-V_s)} \tag{2.8}$$

Rearranging the above equation gives:

$$B=\frac{V_s\cdot T_1}{L}=\frac{V_s\cdot T}{L}\cdot\left(1-\frac{V_s}{E}\right) \tag{2.9}$$

Hence, duty cycle is expressed as follows:

$$D=\frac{T_1}{T}=\frac{E-V_s}{E}=1-\frac{V_s}{E} \tag{2.10}$$

It is apparently shown in Eq. (2.9) that in unipolar PWM scheme either the inductor current error B or the modulation period T, or say the intended switching frequency f, varies with the line voltage V_s, if any of the two parameters mentioned above is kept constant. Similarly, the duty cycle D also varies with the line voltage V_s and cannot be kept as constant in a line cycle to maintain the control over the supply current, see Eq. (2.10).

2.2.2 Proportional-Integral Control

The proportional-integral control scheme[4,19], or PI control, is very similar to proportional control scheme except that the transfer function of the current controller for PI control has a proportional part plus an integral part, see Fig. 2.5. In addition to all the advantages of proportional control, the non-zero steady state current error of proportional control can be eliminated since any difference between the actual current signal and the current reference can be brought to zero by the integral part.

The proportional gain K_p and the integral gain K_i for PI control have to be appropriately

related to prevent the probable instability and to gain the best performance. The determination of the proportional and integral gains requires accurate tuning to suit load parameters [12,19]. Generally, the proportional part determines the speed response and integral part defines the damping factor of the control loop. A fast dynamic response of this control scheme demands a big proportional gain and a small integral gain. If the integral gain is too small, the effectiveness of the integral part decreases, which lowers the feature of the zero steady state current error associated with the integral part. If the proportional gain is too big, the error signal can exceed the amplitude of the triangular waveform, which leads to the subharmonic oscillation problem.

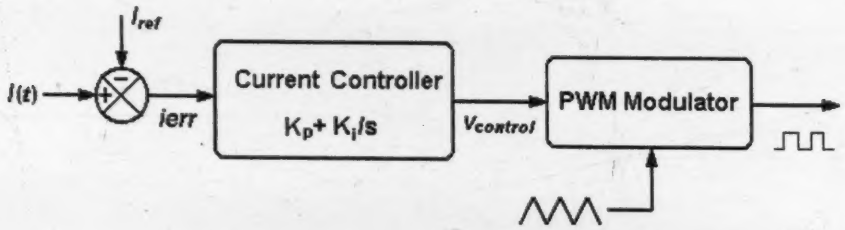


Figure 2. 5 Block diagram of proportional-integral control

For all the current control schemes using a triangular carrier reference, the harmonic distortion of the line current is affected by the amplitude of the triangular waveform [4]. These control strategies are intended to force the current error signal to vary between the maximum and minimum amplitude of the triangular waveform, otherwise the control over the supply current loses. The larger the amplitude of the triangular waveform is, the wider the range of the average current error signal varies, resulting higher harmonic distortion. Accordingly, the amplitude of the triangular carrier should be kept as low as possible.

The lower limit of the amplitude of the triangular carrier is determined by the current error signal. To avoid the multi-switching and consequent disturbances of switch operations, the amplitude of the triangular waveform has to be set so that the slope of the triangular carrier is equal to or greater than the maximum slope of the current error signal.

By observation of Eq. (2.4), Eq. (2.6) and Eq. (2.10), the maximum *di/dt* occurs at the

extreme duty cycle 1 for unipolar PWM, assuming that the peak of the supply voltage is lower than the magnitude of the dc link voltage. Hence:

$$\left.\frac{di}{dt}\right|_{\max} = \frac{E}{L} \tag{2.11}$$

The maximum slope of the triangular carrier waveform could be expressed as follows, referring to Fig. 2.3,

$$\left.\frac{dH}{dt}\right|_{\max} = \frac{H_{\min}/2}{T_{sw}/4} = \frac{2H_{\min}}{T_{sw}} \tag{2.12}$$

Equating Eq. (2.11) and Eq. (2.12), gives:

$$H_{\min} = \frac{E \cdot T_{sw}}{2L} \tag{2.13}$$

Similarly, the minimum amplitude of the triangular carrier for bipolar PWM scheme is expressed as follows, assuming the dc link voltage for bipolar PWM is E:

$$H_{\min} = \frac{E \cdot T_{sw}}{L} \tag{2.14}$$

The maximum current ripple is intended to be less or equal to the half of the minimum amplitude of the triangular waveform. Hence for unipolar PWM, the maximum current ripple is:

$$B_{\max} = \frac{E \cdot T_{sw}}{4L} \tag{2.15}$$

For bipolar PWM scheme, the maximum current ripple is:

$$B_{\max} = \frac{E \cdot T_{sw}}{2L} \tag{2.16}$$

2.2.3 Average Current Mode Control

The average current mode control, or ACMC in short, is originally proposed as an analogue control scheme [5]. The current error is averaged and amplified by the current error amplifier A, as shown in Fig. 2.6. ACMC is of very similar circuit topology with PI control, except the additional capacitor C_p. The controlled current is precisely regulated due to the high gain generated by the current error amplifier [7].

The ramping up slope of the controlled current must not exceed that of the carrier,

otherwise instability occurs [6,7], see Fig. 2.7. This limitation determines the maximum gain of the current amplifier at the switching frequency. The noise immunity of this control scheme is strong [6,7]. This is attributed to the additional pole introduced by capacitor C_p, which is set at the switching frequency to attenuate the effect of noise spikes of the sampled current. No extra slope compensation is required, for the resistor and capacitor networks are specially designed to avoid the occurrence of subharmonic oscillations.

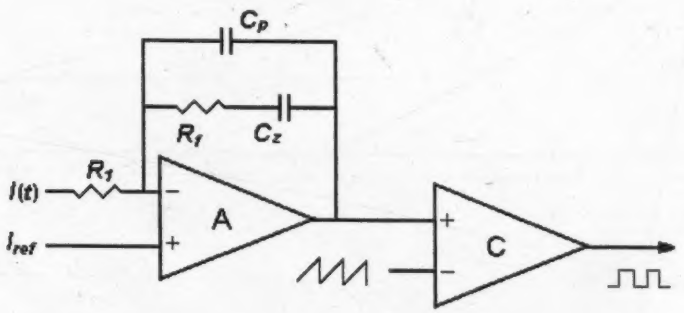


Figure 2. 6 Average current mode control circuit topology

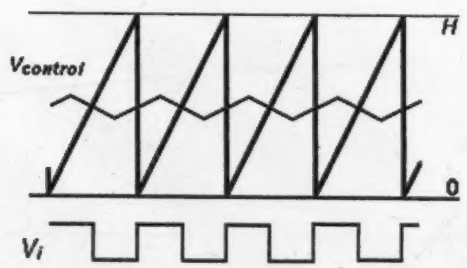


Figure 2.7 Average current mode control waveform

ACMC can be implemented digitally [8,9]. The analogue inductor current signal is sampled and converted to its digital counterpart by a fast ADC at a relatively high frequency so as to ensure the accuracy. The average current I_{ave} is determined by the duty cycle, the maximum and the minimum values of the converted digital current, as shown in Eq. (2.17), rather than being processed by the analogue resistor and capacitor networks.

$$I_{ave} = \left(\left(I_{\min k} + I_{\max k}\right)\cdot D + \left(I_{\max k} + I_{\min k1}\right)\cdot\left(1 - D\right)\right)/2 \qquad (2.17)$$

The major benefit of the digital ACMC is that it eliminates the restriction on the maximum gain at the switching frequency of the current error amplifier for the analogue ACMC. This is because the determination of the duty cycle D does not depend on the cross points of the ramp current signal and the sawtooth waveform. However, the digital scheme introduces the time delay due to the ADC time and the computational time. Cost and complexity are concerned issues for digital ACMC scheme with respect to its analogue version.

2.2.4 Predictive Current Control

Predictive current control [9-14], as implied by its name, is generally a digital control scheme that predicts the voltage control signal [10], the duty cycle [9,11], the inductor voltage [12], the inductor current [13], or the average inverter output voltage [14], at the beginning of every PWM switching period so as to force the supply current to follow its reference precisely at the end of the switching period. The prediction is made on the basis of the intended switching frequency [9-14], the circuit parameter L [9-14], the sampled control variables E, V_s, I_s [9-11], or the estimated line voltage V_s [12-14], according to the bridge operation in previous PWM switching cycles. It is a linear control technique since all the prediction and estimation rely on the linear expression comprised of the intended switching frequency and the sampled or estimated circuit parameters L, E, V_s, I_s.

Generally speaking, the on-line prediction of the desired control variables requires the knowledge of circuit parameters [9-14], which could be either estimated on the basis of a circuit model or sampled through a feedback loop. This makes the prediction either depend more on the circuit model or become more complex due to the increased number of the feedback loop. The prediction, however, provides very accurate control of the inductor current according to its reference, provided the circuit model is accurate enough and does not vary during the work process [14]. The time delay caused by the calculation and ADC or DAC conversion is a common issue of digital control schemes [7,33]. This probably incurs poor dynamic performance in terms of overshoot of the controlled current [12] and relatively slow response

with respect to the analogue scheme [7]. This type of control is mainly categorized into two groups, fixed switching frequency predictive control and deadbeat control [32].

Fixed switching frequency predictive control [9-11] samples and predicts the required control variables only once in a switching period. It samples all the required control variables, estimates the circuit model parameters, and often combines with various control algorithms to accomplish the prediction. For instance, digital ACMC is applied to generate the desired duty cycle at the beginning of the switching period [9]. A sinusoidal modulator is employed, for a voltage control signal is predicted to compare with the triangular carrier to generate the desired duty cycle [10]. Though it is generally a digital control scheme, it could be implemented with an analogue circuitry [11].

Deadbeat control [12-14] detects and updates the control variables twice in one switching cycle. This allows the control routines to be executed twice in one PWM switching period so that the time delay caused by calculation, data conversion, and data propagation could be reduced. It provides relatively faster transient response compared with other digital control scheme, for the time delay in current reference tracking process could be reduced within one PWM switching period [14,33].

2.2.5 Other Reviewed Fixed Switching Frequency Current Control

In addition to P, PI, and ACMC control, current control scheme to realize zero steady state current error of the supply current has been proposed [15]. The transfer function of this current controller is a proportional part plus a second order control part, or say a loss-less digital resonant element by the author. The control goal is achieved by setting the resonant frequency at the line frequency. Consequently the maximum gain for the current error signal is obtained and the minimum average current error is accomplished. By analyzing on its transfer function, it is concluded that no accurate knowledge of the supply voltage and ac side circuit parameters are required for this control scheme. However, the proportional gain and the resonant gain have to be carefully determined to avoid the probable instability [15].

Other research investigations on fixed switching frequency current control concentrate on different modeling techniques using linear or nonlinear control theory [16-19]. Generally, nonlinear PWM rectifiers are modelled and then simplified on the basis of the concept about power balance between the input and the output of rectifier bridges. One approach to handle the nonlinearity is to linearize the model around the operating point based upon the small signal analysis. The controller, consequently, is valid only around the specific operating point, not in the whole operating range [16,19]. Another approach is to develop different modeling technique so as to derive the linear bridge model according to definitions of linear control theory. The controller then is designed by applying the linear control techniques and hence is independent of the operating point [17,18].

2.3 Hysteresis Current Control

Hysteresis current control [1-3,19-31] generates the switching instants directly from the current or voltage error signal by utilizing the hysteresis element. Hysteresis current control basically does not generate immediate voltage control signals to determine switching instants. Consequently, the linearity, which could be described in the form of linear transfer functions, between the control signals and the circuit parameters is lost.

Similarly with fixed switching frequency current control, hysteresis current control has analogue and digital version. For the analogue schemes [1-3,19-21,28-31], the hysteresis band is normally fixed or sinusoidally varied and hysteresis comparators are directly used. For the digital schemes [23-26], the hysteresis band is variable so as to maintain the fixed switching frequency. In this case, the hysteresis comparators are not directly used while similar concept is still adopted.

2.3.1 Fixed Band Hysteresis Current Control

The control concept of fixed band hysteresis control [1,19,20], or tolerance band control [2], is depicted in a block diagram form in Fig. 2.8. It attempts to maintain the current error within

the pre-defined zero-centered fixed hysteresis band through hysteresis comparators, otherwise switching occurs to push the current error back in the opposite direction [1-3,19,20,32,33], see Fig. 2.9. Similar as fixed switching frequency analogue control schemes, either one or two analogue comparators per phase is employed, depending on whether bipolar hysteresis or unipolar hysteresis scheme is adopted [20].

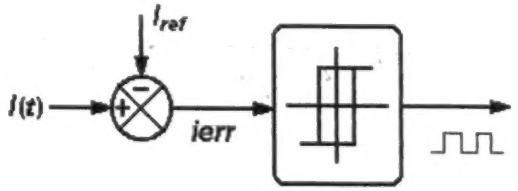
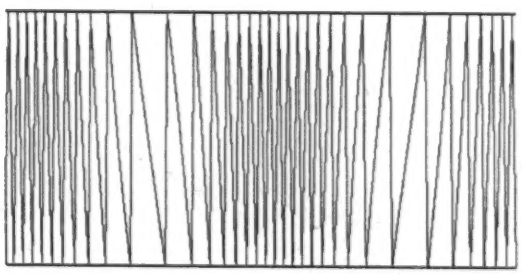
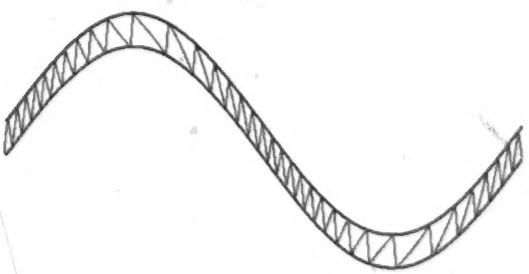


Figure 2.8 Block diagram of fixed band hysteresis control



(a) Current error and fixed hysteresis band



(b) Inductor current and fixed hysteresis band

Figure 2.9 Fixed band hysteresis current control waveforms

Fixed band hysteresis control is a simple and robust control scheme that operates independently from circuit parameter variations [32,33]. The fact that inductor current oscillates

at equidistant away from a centre current reference indicates the lack of tracking errors of this scheme. As a result, an inherent peak current protection is provided [20,21,23]. It also has very good transient response, limited only by switching speed and the line inductance [32]. The simulated characteristics of this control scheme are compared with the proposed control scheme in Chapter 4.

However, the major problem of this control is the variable switching frequency [2,3,19,21,32,33]. It brings in a large amount of low order harmonics and a broad range of switching frequency, resulting in high stress on the electronic equipment, high switching losses, overheating problem, and increased difficulties on the design of low order harmonic filters [2,21,33]. The switching frequency depends largely on the line inductance and varies with the ac supply voltage [19,23,32]. Referring to Eq. (2.25), the maximum switching frequency for bipolar hysteresis control occurs around the zero crossing of the supply voltage and is estimated in Eq. (2.18).

$$f_{max} = \frac{E}{4 \cdot L \cdot B} \tag{2.18}$$

The minimum switching frequency for bipolar hysteresis control occurs at the crest of the ac supply voltage and is approximately given in Eq. (2.19), assuming V_s equal to $0.9 \cdot E/2$. In this case, the maximum switching frequency is more than five times the minimum switching frequency.

$$f_{min} = \frac{0.19 \cdot E}{4 \cdot L \cdot B} \tag{2.19}$$

For the single-phase PWM rectifier with bipolar PWM control scheme, assume the supply voltage is invariable in every switching cycle and the supply current error is well regulated within the $+B/2$ to $-B/2$ current band, as shown in Fig. 2.4. According to Eq. (1.7), the switch on-time T_1 is expressed as:

$$L\frac{B/2 + B/2}{T_1} = V_s + E/2 \tag{2.20}$$

Rearranging the above equation yields:

$$T_1 = \frac{L \cdot B}{V_s + E/2} \tag{2.21}$$

Similarly, for the switch off-time T_2, it has:

$$L\frac{-B/2 - B/2}{T_2} = V_s - E/2 \tag{2.22}$$

Rewriting the above equation, gives:

$$T_2 = \frac{-L \cdot B}{V_s - E/2} \tag{2.23}$$

The switching period is the sum of the switch on-time T_1 and the switch off-time T_2,

$$T = T_1 + T_2 = \frac{L \cdot B}{V_s + E/2} + \frac{-L \cdot B}{V_s - E/2} = \frac{L \cdot B \cdot E}{E^2/4 - V_s^2} \tag{2.24}$$

Rewriting the above equation gives the switching frequency:

$$f = \frac{E^2/4 - V_s^2}{L \cdot B \cdot E} \tag{2.25}$$

Rewriting Eq. (2.22) again gives:

$$B = \frac{\left(E^2/4 - V_s^2\right) \cdot T}{L \cdot E} \tag{2.26}$$

Hence, duty cycle is expressed as follows:

$$D = \frac{T_1}{T} = \frac{E/2 - V_s}{E} \tag{2.27}$$

It is apparently shown in Eq. (2.26) that in bipolar PWM scheme either the inductor current error B or the modulation period T, or say the intended switching frequency f, varies with the line voltage V_s, if any of the two parameters mentioned above is kept constant. Similarly, the duty cycle D also varies with the line voltage V_s and cannot be kept as constant in a line cycle to maintain the control over the supply current, see Eq. (2.27).

2.3.2 Sinusoidal Band Hysteresis Current Control

Sinusoidal band hysteresis current control [20-22] is intended to reduce the high amount of

harmonics produced by fixed band hysteresis control while maintaining all its benefits without increasing the implementation complexity. The block diagram of this control is depicted in Fig. 2.10.

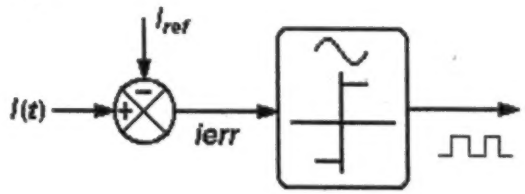
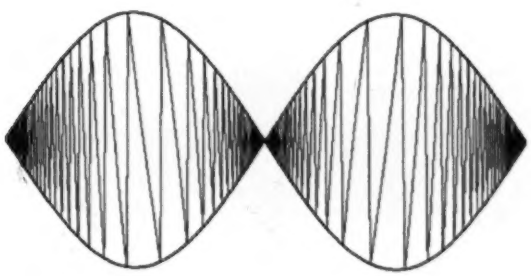
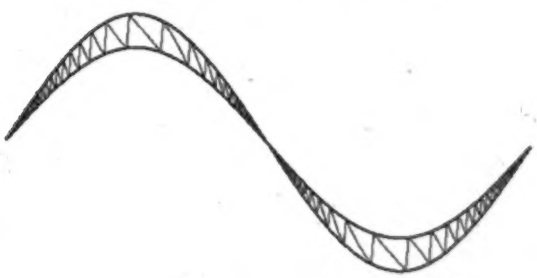


Figure 2.10 Block diagram of sinusoidal band hysteresis control



(a) Current error and sinusoidal hysteresis band



(a) Inductor current and sinusoidal hysteresis band

Figure 2.11 Sinusoidal band hysteresis current control waveforms

As implied by its name, instead of the fixed hysteresis band, the current error is regulated to vary within a sinusoidal-shaped zero-centered hysteresis band during a line cycle, see Fig. 2.11. This contributes to less harmonic distortion compared with fixed band hysteresis control

scheme [21,22]. However, the pretty small magnitude of the sinusoidal hysteresis band around zero crossing points results in even higher average and maximum switching frequency of this control scheme compared to fixed band hysteresis control [21,22]. This scheme could be implemented in either unipolar hysteresis or bipolar hysteresis scheme [20].

To obtain a trade-off between the switching frequency variations and the harmonic distortions, mixed band hysteresis control [22] has been proposed. The block diagram of this control scheme is shown in Fig. 2.12. This control scheme simply mixes the sinusoidal hysteresis band and the fixed hysteresis band together so that the high switching frequency around zero crossing is limited by the fixed amplitude of the current error band. On the other hand, the large amount of harmonics is reduced due to the sinusoidal-shaped current error band. Design is required based upon the specification of the controller to determine the magnitudes of the fixed and sinusoidal hysteresis bands.

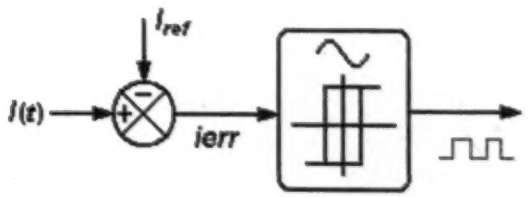


Figure 2.12 Block diagram of mixed band hysteresis control

2.3.3 Delta Modulation Control

Delta modulation control [28-31], or DM in short, is a generic modulation technique that converts analogue signal into PWM digital signal using hysteresis comparators. It is also known as model reference adaptive control, or MRA [31].

To produce the digital output pulses for DM control, the reference signal V_R is compared with the integral of the output pulses V_F by means of a hysteresis element, as shown in Fig. 2.13. The function of the integrator is to generate the analogue signal V_F with the digital pulses as an input. The close loop structure of the DM controller ensures that the polarity of the output pulses is adjusted by the sign of the error signal. The analogue signal V_F is allowed to oscillate

within a pre-defined hysteresis band that is centered on the reference signal V_R. The switching occurs whenever the V_F intersects with the reference V_R, forcing V_F to oscillate around V_R [28,29].

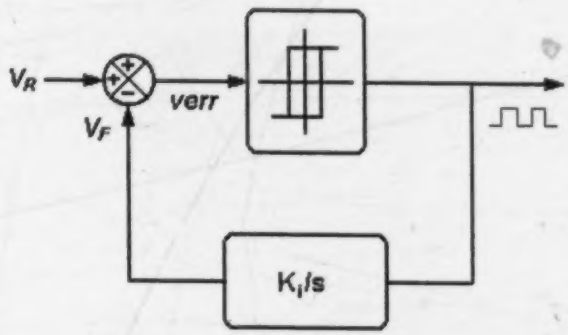


Figure 2.13 Block diagram of delta modulation control

The above description of DM controller reveals that this is a hysteresis control scheme. It is similar as fixed band hysteresis control, for the oscillation of the analogue signal is restricted within a hysteresis band. In this sense, the switching instant of the free running bridge is possible to occur at any time instant [31]. It is inherently stable, since the subharmonic issue of the carrier-based control scheme is successfully avoided by this scheme. On the other hand, the excursion of the switching frequency of this scheme could be limited within a relatively narrow range with respect to fixed band hysteresis control. This is accomplished by a careful design on the gain of the integrator associated with a suitable hysteresis band value.

However, in addition to the variable switching frequency problem, phase jitter of the output signal is another issue of this scheme. Phase jitter occurs when the fundamental harmonic of the PWM output waveform experiences cycle-to-cycle phase shifts. This is caused by switching edges of the PWM waveform occurring at different position in the fundamental cycle. Phase jitter could be eliminated provided the ratio between the expected switching frequency and the line frequency is high enough [31].

Control schemes based upon DM with improved performance are reported [30,31]. The

attempts are made to gain the constant switching frequency and to eliminate the occurrence of the possible phase jitter. One method is to introduce a fixed frequency synchronizing pulses so as to determine the corresponding hysteresis band that could eliminate the phase jitter [30]. Another approach [31] is to develop a mixed signal by imposing a small magnitude constant frequency triangular carrier on the sinusoidal reference signal V_R. The mixed signal then is compared with the analogue signal V_F to generate the output pulses, as shown in Fig. 2.14. Instead of the original scheme, the analogue signal V_F oscillates within the band determined by the imposed triangular carrier. The constant switching frequency is achieved since the switching is determined by the intersection of the mixed signal and analogue signal V_F.

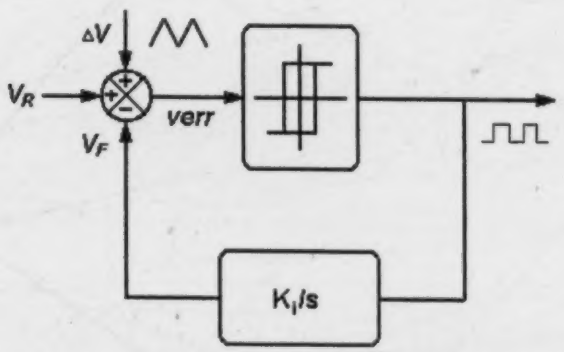


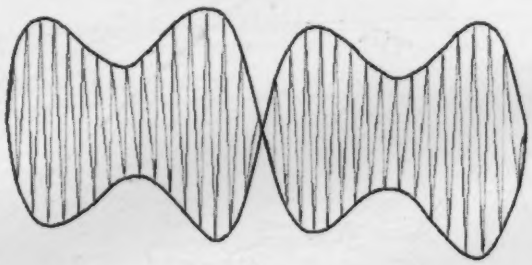
Figure 2.14 Block diagram of improved delta modulation control

2.3.4 Variable Band Hysteresis Current Control

In an attempt to obtain the constant switching frequency on the basis of the hysteresis algorithm, variable band hysteresis control scheme is proposed [23-25]. This scheme attempts to generate the desired variable hysteresis band, see Fig. 2.15, which could provide fixed switching frequency on the basis of either measured circuit parameters [23,24] or detected zero crossing points of the current error signal [25]. For the former, it shares the similar problem with predictive current control introduced in section 2.2.4, for both schemes employs the on-line prediction that requires the knowledge of circuit parameters.

An adapted hysteresis current control [25] is studied in detail in this section, whose

hysteresis band is chosen based upon the detected current error zero crossing, the intended switching frequency, and the previous hysteresis band values. The fixed switching period $2T$ has a corresponding constant hysteresis band B, as shown in Fig. 2.16. The control goal is to generate a desired variable hysteresis band that could push the current error zero crossing to the desired fixed points to maintain the constant switching frequency.



(a) Current error and variable hysteresis band

(a) Inductor current and variable hysteresis band

Figure 2.15 Variable band hysteresis current control waveforms

If the upper hysteresis band B_{p0} in switching cycle k0 goes beyond the desired band value, as shown in Fig. 2.16, the current error zero crossing deviates from the intended fixed point and time error t_{ep0} is detected. For the same reason, time error t_{en0} occurs due to the lower hysteresis band B_{n0} beyond the desired band B. The upper hysteresis band B_{p1} in switching cycle k1 is determined so as to force the current error reaches the desired zero crossing. The lower hysteresis band B_{n1} in the same switching cycle k1 is generated separately, allowing two updates of the control routine so as to guarantee the fast deadbeat response.

This digital-based control scheme has very good performance in terms of successfully

achieved fixed switching frequency, accurate control in inductor current, low harmonic distortions, fast deadbeat response, and high immunity of circuit parameters variations. Due to the analogy, it is selected to compare with the proposed slope detective current control in Chapter 4. The detailed formula derivation of this scheme is introduced in this section and the simulation characteristics are presented in Chapter 4. Only the determination of upper hysteresis band B_{pl} is derived to clarify the control concept. A totally symmetrical expression for the lower hysteresis band B_{nl} could be derived in the similar way and is omitted here.

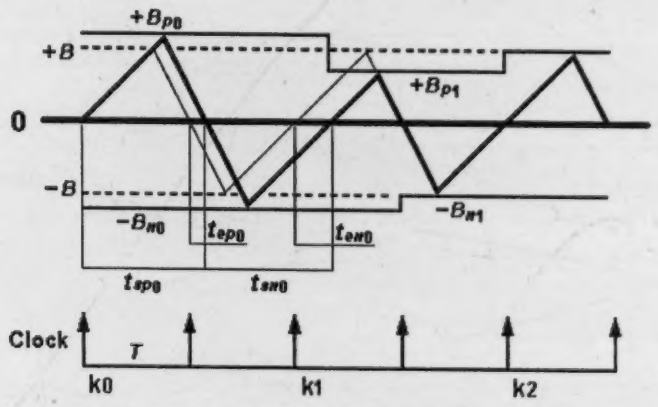


Figure 2.16 Principle of variable band hysteresis control

By observation of Fig. 2.16, time error t_{ep0} and t_{en0} are described in Eq. (2.28) and (2.29),

$$t_{ep0} = t_{sp0} - T \tag{2.28}$$

$$t_{en0} = t_{sn0} + t_{ep0} - T \tag{2.29}$$

Also, Eq. (2.30), Eq. (2.31), and Eq. (2.32) are written assuming that the switching frequency is high enough so that the inductor current error is ramping linearly in every switching period,

$$\frac{t_{sn0}}{t_{sp0}} = \frac{B_{n0}}{B_{p0}} \tag{2.30}$$

$$\frac{B}{T} = \frac{B_{p0}}{t_{sp0}} \tag{2.31}$$

$$\frac{B}{T} = \frac{B_{p1}}{T - t_{en0}} \tag{2.32}$$

Equating Eq. (2.31) and (2.32) gives,

$$B_{p1} = \frac{B_{p0} \cdot (T - t_{en0})}{t_{sp0}} \tag{2.33}$$

Substituting Eq. (2.29) and Eq. (2.30) into Eq. (2.33) yields,

$$B_{p1} = \frac{B_{p0}}{t_{sp0}} \cdot \left(2T - t_{ep0} - \frac{B_{n0}}{B_{p0}} \cdot t_{sp0} \right) \tag{2.34}$$

In the above equation, time error t_{ep0} and time value t_{sp0} between the two zero crossing time instants can be measured. The positive and negative hysteresis bands B_{p0} and B_{n0} in the previous switching cycle k0 are known with respect to switching cycle k1. In this sense, the desired positive hysteresis band B_{p1} can be determined according to Eq. (2.34).

2.3.5 Zero Average Current Error Control

Zero average current error control [26,27], or ZACE in short, is a digital current control scheme that attempts to force the average current error to be zero in every switching cycle. To achieve this, the negative excursion area A− is forced to match the most recent positive excursion area A+ in the same switching period, as shown in Fig. 2.17. As a result, the supply current is precisely controlled to follow the current reference so that low order harmonics are eliminated by the control scheme during the line cycle.

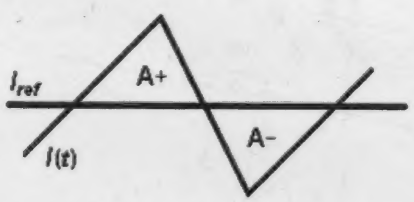


Figure 2.17 Current error signal under ZACE control

Based upon this control concept, two control algorithms are proposed to accomplish the

control goal. The block diagram of slope generated hysteresis current control [26], or SGH, is shown in Fig. 2.18. The control algorithm attempts to generate the desired variable hysteresis band on the basis of the current error slope together with the intended switching frequency so as to maintain the constant switching frequency. The positive and negative hysteresis bands are set at half of the calculated band value in order to achieve ZACE in each switching period.

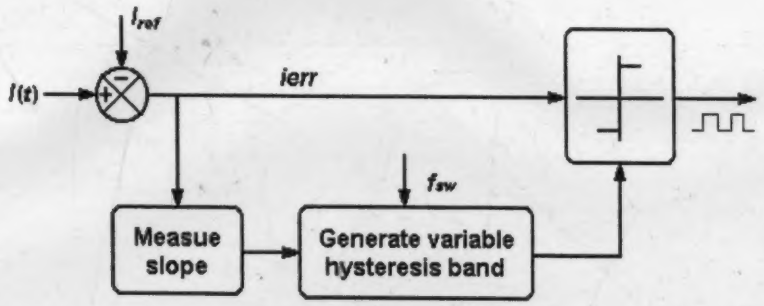


Figure 2.18 Block diagram of slope generated hysteresis control

Ramptime current control [27] accomplishes ZACE relying only on the detection of the zero crossing instants of the current error signal, without producing the expected variable hysteresis band or requiring the magnitude of the current error signal. The scheme is explained by reference to the current error waveform in Fig. 2.19.

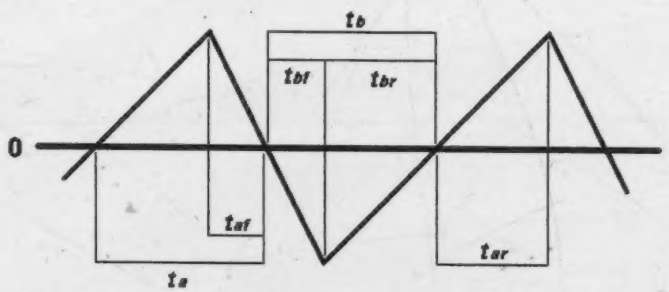


Figure 2.19 Principle of ramptime control

The bridge is free running during period t_{af} until it reaches the zero crossing point. The successive following period t_{bf} is generated based upon t_{af}, t_a, and the intended switching

frequency together in a digital logic, which is intended to obtain equal period t_a and t_b. Once period t_{bf} is chosen, the corresponding switching instant is also determined. In the samilar way, period t_{ar} and the corresponding switching instant are determined. In this manner, the switching instants are continuously generated. ZACE is accomplished by forcing the current error signal to have equal periods in its positive and negative half cycle, see t_a and t_b in Fig. 2.19, provided the switching frequency is high enough so that the inductor current error is assumed ramping linearly in every switching cycle.

ZACE control produces fairly accurate control and negligible low order harmonic distortions with respect to other control schemes [26,27]. The regulation over the supply current of this control is independent of changes in circuit parameters. It also has relatively fast transient response. However, it shares the time delay problem with other digital control schemes. The control accuracy of both schemes is degraded by the time delay issue [26,27].

For ramptime control, the requirement for the precise measurement on the time duration between the switching instant and the zero crossing point is pretty strict [27]. For SGH control, the supply current overshoots its reference during the transient response. In addition, it is prone to the noise problem caused by the differentiators used to determine the ramp rates [26]. Moreover, inaccuracy of this control is introduced by the filtration required to remove the noise from the current error slope measurement [27].

2.4 Summary

Current control techniques are primary catalogued into two groups, fixed switching frequency current control and hysteresis current control. Current control techniques reviewed and discussed in this chapter have been introduced as background knowledge to the work presented in this thesis.

Fixed frequency current control has the merits of a constant switching frequency and consequently low switching losses and low harmonic distortions. However, for the analogue-based fixed switching frequency control schemes, the control accuracy is less

satisfying. For the digital-based fixed switching frequency control schemes, precise control could be achieved. However, most predictive current control algorithms require the knowledge of circuit parameters to predict the desired switching instant, resulting in poor performance in case of circuit parameters variations.

Hysteresis current control schemes are inherently stable and robust [32,33]. Zero-centered current error, fast transient response and peak current protection are merits of these control schemes. However, for the analogue-based hysteresis control schemes, large variations of the switching frequency exist, producing a large amount of harmonic distortion and high switching losses. For the digital-based hysteresis control schemes, efforts are put into maintaining a constant switching frequency while variations of the switching frequency cannot be totally eliminated, especially in practical applications.

Due to the various limitations of all existing current control schemes, new efforts are continuously being put into seeking new current control schemes. Sloped detective current control is proposed in this thesis. This control scheme is a digital-based fixed switching frequency unipolar PWM current control scheme that achieves a symmetrical zero-centered current error in the inductor current. The desired switching instant is predicted based upon the sampled slopes of the current error signal in the previous two successive switching cycles. No circuit parameters are required to determine the intended switching instant, excluding the current feedback loop. In addition to all the merits of the digital-based fixed switching frequency current control schemes, the proposed scheme has high immunity to circuit parameters mismatches, ac supply voltage distortions and dc link voltage variations. Accurate, and stable regulation of the inductor current can be achieved by the proposed scheme.

Chapter 3 Model-Based Predictive Current Control

Model-based predictive current control scheme proposed in this chapter is a constant frequency unipolar PWM control algorithm that achieves a symmetrical zero-centered current error in every switching cycle. Based upon the pre-determined circuit model of the single-phase PWM rectifier bridge, the desired switching instants are continuously generated so that the supply current is regulated to follow its current reference precisely. Since all the information required for the prediction of the switching instants is generated by using the circuit model, no feedback is necessary for this control scheme.

The intuitive descriptions and the basic concepts of the proposed control scheme are introduced first. The advantages and disadvantages of the proposed control scheme are qualitatively discussed, and illustrated using simulated results from a single-phase PWM rectifier topology. In addition, relevant formulas that lead to the quantitative analysis are also presented in this chapter.

3.1 General Description

The basic control concept of ***model-based predictive current control scheme*** is depicted in Fig. 3.1. As described by its name, this control scheme is intended to choose the suitable switching instants based upon assumed values for the circuit model parameters rather than the real-time measurement of the actual parameters. Consequently, no feedback loop is necessary to accomplish the control goal.

The proposed control scheme is a constant frequency control scheme without using a triangular carrier reference to generate the PWM output pulses. The switching frequency of the scheme is determined by the fixed clock rate provided by digital equipment or any integrated circuit chip. In this scheme, the start time instant t_0 and the end time instant t_2 are two significant time instants in a PWM switching cycle as shown in Fig. 3.2. These two time

instants are determined by the intended switching frequency and represent the start and end points of a PWM switching cycle.

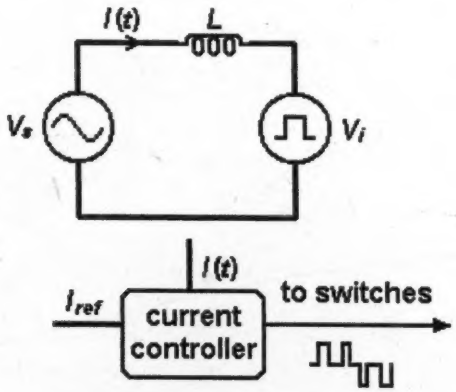


Figure 3.1 Block diagram of model-based predictive current control

A key issue of precise current waveshaping PWM controllers is how to force the actual current to follow the pre-established current reference trajectory with a constant switching period and a minimum current error being generated. The desired PWM pattern is developed by turning on and turning off the power transistors of the rectifier bridge at the switching frequency. Both bipolar PWM and unipolar PWM produce two voltage states, high or low relative to each other in each switching cycle The PWM pattern with its two voltage states in each switching cycle is modelled as a modulated voltage source. This modulated voltage source V_i, together with the supply voltage source V_s and the induced voltage across the inductor V_L, establishes an instantaneous dynamic balance in the voltage loop, as shown in Fig. 3.1.

The induced voltage across the inductor V_L balances the difference between the supply voltage V_s, and the modulated voltage V_i. The current through the inductor, namely the supply current, varies according to this difference. Due to the two voltage states of the modulated voltage source V_i, the induced voltage across the inductor V_L jumps dramatically one time in every switching cycle. Accordingly, the supply current ramps upward as long as the supply voltage is higher than one state of the modulated voltage, while ramping downward when the

supply voltage is lower than the other state of the modulated voltage in the same switching period.

The current error is the difference between the actual current signal and the current reference. The function of the current error signal is designated as $ierr_1(t)$ and $ierr_2(t)$ respectively in Fig. 3.2. For a successful control, the current error must have positive values and negative values. Moreover, it must have positive ramping rate and negative ramping rate respectively in one PWM switching cycle to keep the control over the supply current, though the ramping rate values are not necessary to be the same. The two distinct segments of the current error in Fig. 3.2 are expected to occur in every switching cycle as the result of all control algorithms and could be expressed in the manner of formulas associated with the circuit model parameters. Since the start time instant and the end time instant of every switching cycle are always fixed and known for this scheme, the control targets its goal at choosing the intended switching instant t_1 between t_0 and t_2.

The intention of the control algorithm is to accomplish the symmetrical zero-centered current error in every switching cycle. In other words, the basic control law can be said to be forcing $ierr_2(t_2)$ to be the same as $ierr_1(t_1)$, as shown in Fig. 3.2. The switching instant t_1 is determined according to the circuit model in conjunction with this current control law, for all the circuit parameters are known at the time when the rectifier bridge is modelled.

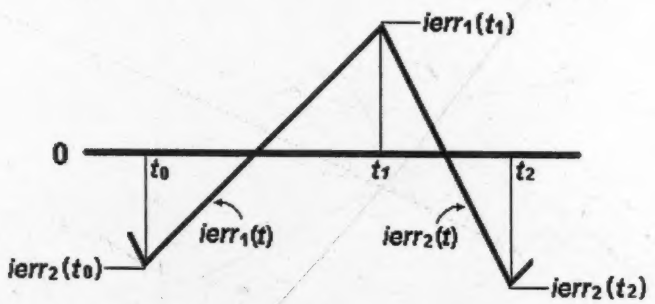


Figure 3.2 Current error waveform under model-based predictive control

The proposed model-based predictive current control scheme achieves the symmetrical

zero-centered current ripple provided the circuit running environment matches the pre-established circuit model. It works independently from the real-time measurement of the actual parameters so that no feedback loop is essential for this scheme. It presents unity PF performance combined with unipolar PWM scheme at a relatively low switching frequency, which indicates lower switching losses and higher efficiency.

The proposed control scheme loses the precise control over the supply current when the actual circuit does not function under the same working conditions assumed for modelling the circuit. The apparent excursions of the average current error occur under circuit parameters variations since the determination of the switching instant relies on the circuit parameters. This weakness applies to all predictive control schemes that generate the PWM output pulses with the knowledge of circuit parameters. Besides, since no feedback loop is required for this scheme, the control over the supply current is lost if noise or supply voltage fluctuations is severe. The zero crossing of the supply voltage can introduce apparent deviations in the average current error, an effect very commonly associated with unipolar PWM scheme [4,20]. Further detailed discussion about this issue is provided in section 3.4.

This control scheme has a potential to be implemented in the specially designed analogue circuits, provided the improvement of the scheme is developed and the current feedback loop is included. This issue is discussed in section 3.3. In this thesis, this control scheme is introduced and examined as the origination and foundation of a more refined control scheme described in Chapter 4.

3.2 Formula Derivation

The proposed control algorithm is developed upon the most basic formula in Eq. (1.6), which reveals the operation of the single-phase PWM rectifier. In this section, the deductive procedure from this basic equation to the final formulas for the proposed scheme is introduced. In addition to the detailed formula derivations, several significant concepts and relevant interpretations are stated.

3.2.1 Basic Formulas

As mentioned in Chapter 1, the proposed current control scheme in this thesis has its operation based upon unipolar PWM scheme with the simplified model. Rewriting the expressions given in Chapter 1 for the supply voltage source V_s, and the modulated voltage source V_i, respectively, gives:

$$V_s = V_{pk} \sin \omega t \tag{3.1}$$

$$V_i = \begin{Bmatrix} 0 \\ sign(V_s) \cdot E \end{Bmatrix} \tag{3.2}$$

The differences between the supply voltage source V_s and the modulated voltage source V_i is instantaneously balanced by the induced voltage across the inductor L. Therefore,

$$V_L = V_s - V_i \tag{3.3}$$

Substituting Eq. (3.2) into Eq. (3.3) gives:

$$L\frac{di}{dt} = V_s - V_i = \begin{Bmatrix} V_s \\ V_s - sign(V_s) \cdot E \end{Bmatrix} \tag{3.4}$$

Rearranging and substituting Eq. (3.1) into the above equation, yields:

$$di = \frac{V_s - V_i}{L} dt = \begin{Bmatrix} \frac{V_s}{L} dt \\ \frac{V_s - sign(V_s) \cdot E}{L} dt \end{Bmatrix} = \begin{Bmatrix} \frac{V_{pk} \sin \omega t}{L} dt \\ \frac{V_{pk} \sin \omega t - sign(V_s) \cdot E}{L} dt \end{Bmatrix} \tag{3.5, 3.6}$$

3.2.2 Expressions of the Supply Current

The modulated voltage source V_i produces a PWM pattern with three possible states, $+E$, 0, $-E$. During every switching cycle, only two states, either 0 and $+E$, or 0 and $-E$, are produced to make the supply current ramping up and down around the current reference, I_{ref}. The ramping up process starts from time instant t_0 with the initial current value of I_0, as illustrated in Fig. 3.3. The ramping up process reaches its peak current value I_1 in this switching cycle at switching instant t_1. The current ramps in the opposite direction and goes to the end time instant t_2 of this

switching cycle with its value I_2. The time instants t_0 and t_2 are fixed points so as to ensure the constant switching frequency as a feature. The control effort is to predict a suitable switching instant, namely time instant t_1, such that the combination of the two current ramping activities delivers the minimum harmonics in the controlled supply current.

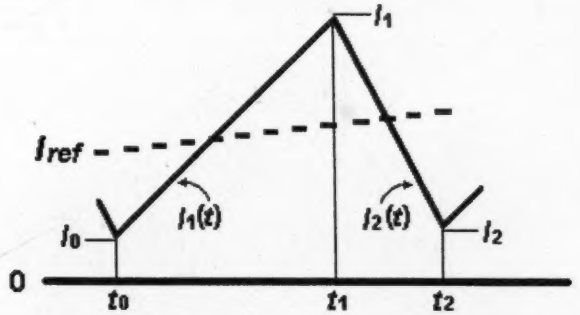


Figure 3.3 Supply current waveform in one PWM switching cycle

The expression of the inductor current in the "zero-voltage" state of the modulated pulse voltage is derived by integrating both sides of Eq. (3.5).

$$I_1(t) = -\frac{V_{pk}}{\omega L}(\cos\omega t - \cos\omega t_0) + I_0 \tag{3.7}$$

Hence, the peak current value I_1 is expressed as follows:

$$I_1 = I_1(t_1) = -\frac{V_{pk}}{\omega L}(\cos\omega t_1 - \cos\omega t_0) + I_0 \tag{3.8}$$

Similarly, the expression of the inductor current in the "high-voltage" state of the modulated pulse voltage in the same switching cycle can be derived by integrating both sides of Eq. (3.6), which further gives the current value I_2 of the end time instant t_2 of the switching period:

$$I_2(t) = -\frac{V_{pk}}{\omega L}(\cos\omega t - \cos\omega t_1) - \frac{sign(V_s)\cdot E\cdot(t - t_1)}{L} + I_1 \tag{3.9}$$

$$I_2 = I_2(t_2) = -\frac{V_{pk}}{\omega L}(\cos\omega t_2 - \cos\omega t_1) - \frac{sign(V_s)\cdot E\cdot(t_2 - t_1)}{L} + I_1 \tag{3.10}$$

3.2.3 Concepts and Formulas of the Current Error

The current error, a difference between the actual current and the current reference, is a control variable that deserves the most concern of all control schemes. The zero current error indicates that the actual controlled current exactly follows the current reference at any time instants. Although an instantaneous zero current error is impossible to achieve in reality, it is the goal for all the current control schemes to minimize the average current error as much as possible.

The current reference, namely the current template, should be with the same shape and in phase with the supply voltage to produce a unity PF of the supply current. An expression for the current reference is as follows:

$$I_{ref} = I_{pk} \sin \omega t \tag{3.11}$$

For this control scheme, the two current error expressions for the first ramping process and the second ramping process in each switching cycle are given by subtracting the actual current expressions from its reference. Hence the current error in the first ramping process is described as follows,

$$ierr_1(t) = I_1(t) - I_{ref} \tag{3.12}$$

Substituting $I_1(t)$ in Eq. (3.7), and I_{ref} in Eq. (3.11) in Eq. (3.12) respectively, gives,

$$ierr_1(t) = -\frac{V_{pk}}{\omega L}(\cos \omega t - \cos \omega t_0) + I_0 - I_{pk} \sin \omega t \tag{3.13}$$

Therefore, the current error value at the switching instant t_1, see Fig. 3.2, is,

$$ierr_1(t_1) = -\frac{V_{pk}}{\omega L}(\cos \omega t_1 - \cos \omega t_0) + I_0 - I_{pk} \sin \omega t_1 \tag{3.14}$$

Likewise, the current error in the second ramping process in one PWM cycle is given as,

$$ierr_2(t) = I_2(t) - I_{ref} \tag{3.15}$$

Substituting $I_2(t)$ in Eq. (3.9), and I_{ref} in Eq. (3.11) in Eq. (3.15) respectively, yields,

$$ierr_2(t) = -\frac{V_{pk}}{\omega L}(\cos\omega t - \cos\omega t_1) - \frac{sign(V_s)\cdot E\cdot(t-t_1)}{L} + I_1 - I_{pk}\sin\omega t \qquad (3.16)$$

Hence, the current error value at the end time instant t_2, see Fig. 3.2, is:

$$ierr_2(t_2) = -\frac{V_{pk}}{\omega L}(\cos\omega t_2 - \cos\omega t_1) - \frac{sign(V_s)\cdot E\cdot(t_2-t_1)}{L} + I_1 - I_{pk}\sin\omega t_2 \qquad (3.17)$$

The current control law of this proposed control scheme is to obtain the symmetrical zero-centered current error in every PWM switching period. In other words, the two instantaneous current errors, $ierr_1(t_1)$ and $ierr_2(t_2)$, are expected to be equal on the amplitudes with opposite polarities at every single switching cycle,

$$ierr_1(t_1) = -ierr_2(t_2) \qquad (3.18)$$

Substituting Eq. (3.14) and Eq. (3.17) into Eq. (3.18), gives,

$$-\frac{V_{pk}}{\omega L}\cos\omega t_1 - I_{pk}\sin\omega t_1 + sign(V_s)\cdot\frac{E}{L}t_1$$

$$= -\frac{V_{pk}}{\omega L}(2\cos\omega t_0 - \cos\omega t_2) + sign(V_s)\cdot\frac{E}{L}t_2 - 2I_0 + I_{pk}\sin\omega t_2 \qquad (3.19)$$

In Eq. (3.19), t_0 and t_2 are fixed frequency time instants that are known as long as the switching frequency is determined. I_0, the initial current value of the present switching cycle, is actually the current value of the end time instant of the previous successive switching cycle, which is also known. As for the other circuit parameters in the equation, such as V_{pk}, I_{pk}, E, L, are known as the PWM rectifier bridge has been modelled. Solving the equation, the only unknown variable t_1 is obtained. In this sense, the switching instant of every single switching period can be determined based upon the control law defined in Eq. (3.18).

However, Eq. (3.19) is not a linear equation for solving the switching instant t_1. Besides, it does not present the direct solution for t_1, indicating that it is not suitable for the real-time calculation purpose. Modifications on this control scheme can lead to the other proposed control scheme that is described in Chapter 4.

3.3 MATLAB Program Description

All the simulation programs in this thesis are fulfilled by MATLAB and are attached in the appendix for detailed references. For all MATLAB programs in this thesis, there are no physical analogue components involved to emulate the single-phase PWM rectifier bridge. Instead, a model is developed to represent the operation of the single-phase PWM rectifier for the simulation purpose, see Fig. 1.2. Consequently, relevant mathematic formulas, such as the inductor current in Eq. (3.7) and Eq. (3.9) and the current error in Eq. (3.13) and Eq. (3.16), are adopted. The MATLAB program for model-based predictive current control scheme is attached in appendix A.

$$K(t_0,t_2)=-\frac{V_{pk}}{\omega L}(2\cos\omega t_0-\cos\omega t_2)+sign(V_s)\cdot\frac{E}{L}t_2-2I_0+I_{pk}\sin\omega t_2 \quad (3.20)$$

$$F(t)=-\frac{V_{pk}}{\omega L}\cos\omega t-I_{pk}\sin\omega t+sign(V_s)\cdot\frac{E}{L}t \quad (3.21)$$

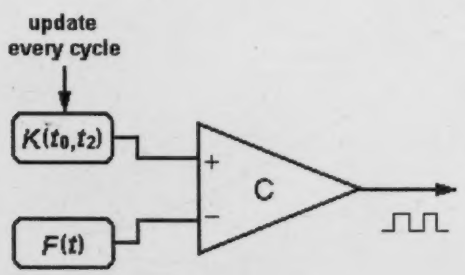


Figure 3.4 Determination of switching instants by MATLAB program

By separating Eq. (3.19) and introducing two new variables $K(t_0, t_2)$ and $F(t)$, Eq. (3.20) and Eq. (3.21) are obtained. For variable $K(t_0, t_2)$, it gets updated at the beginning of every switching cycle. In other words, the value of this variable is always known for all PWM switching cycles. For the other variable $F(t)$, it is capable in MATLAB program to further divide each switching cycle into more shorter time intervals to compute the corresponding variable values. Since no linear expression for the intended switching instants could be derived

for this scheme, an alternative method with the analogy of an analogue comparator is adopted, as shown in Fig. 3.4. Once values of the two variables $K(t_0, t_2)$ and $F(t)$ are within the pre-defined precision region, the corresponding switching time instants t_1 in Eq. (3.19) is obtained.

The MATLAB program of this control scheme exhibits a potential for this control scheme to be implemented by the sophisticatedly designed analogue circuits. Comparators, multipliers, sine and cosine function generators, and fixed clock rate generators, etc, could be employed to realize the control scheme. However, improvement of this control scheme to suit for practical application by involving the current feedback loop and increasing immunity of circuit parameters variations is necessary before the practical implementation.

3.4 Simulated Characteristics

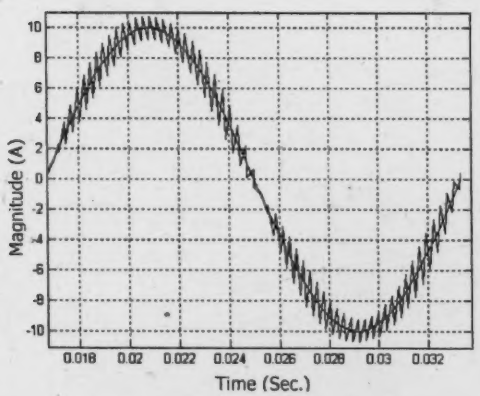
Model-based predictive current control scheme is investigated using the single-phase PWM rectifier to verify the effectiveness of the control algorithm. The simulations undertaken on MATLAB program are developed to have the effectiveness of the control algorithm investigated under the conditions that emulate the practical experimental environment, such as the inductance mismatch between the circuit and the model; the random noise imposed on the ac supply voltage, and the second harmonic injected in the dc link voltage.

3.4.1 Simulation Under the Nominal Condition

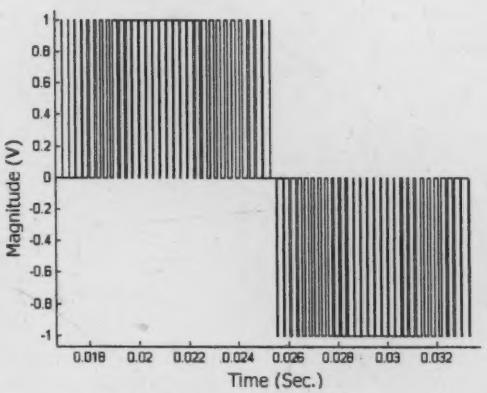
The simulation waveforms of the proposed scheme under the nominal condition are shown in Fig. 3.5. The inductor current is precisely controlled to follow the current reference. The proposed algorithm achieves zero-centered current error combined with unipolar PWM scheme, provided the circuit parameters match the model parameters, as listed in Table 3.1. The average current error is obtained by averaging the magnitudes of the two opposite peak current errors during every PWM switching cycle. Though it is not a strict technique to define the average current error, this approach produces simple and straightforward approximation.

Table 3.1 Circuit parameters of simulation waveforms in Fig. 3.5

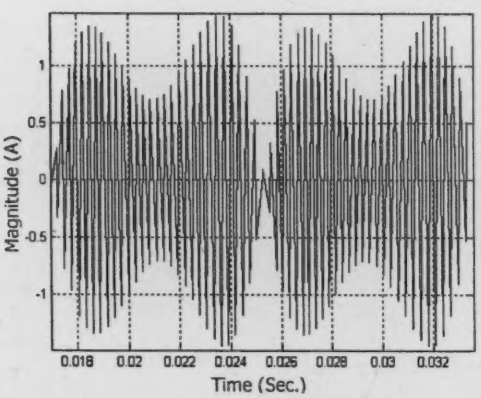
Parameters	Circuit Values	Model Values
Supply Inductance (L)	5mH	5mH
Supply Voltage (V_{pk})	169V, 60Hz	169V, 60Hz
dc Link Voltage (E)	200V	200V
Switching Frequency (f_{sw})	1800Hz	Not required
Clock Frequency	3600Hz	Not required
Current Reference (I_{ref})	10A	10A



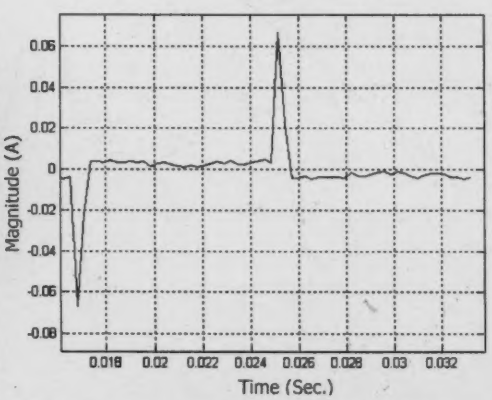
(a) Supply current and its reference



(b) Unipolar voltage switching pulses

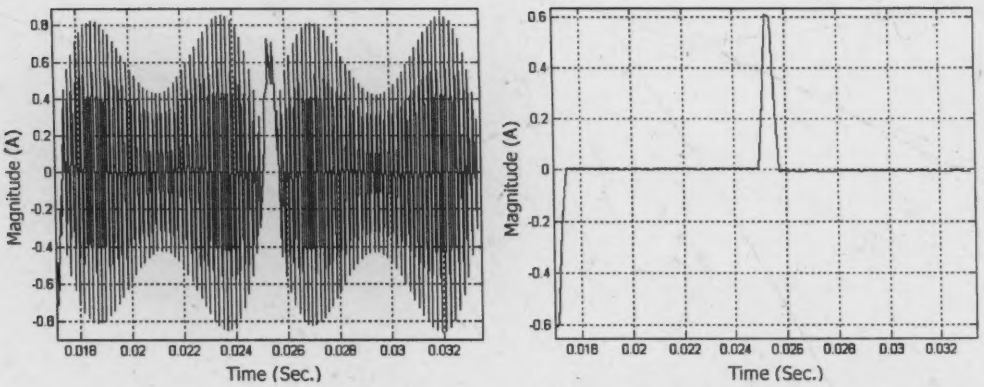


(c) Current error in a switching cycle



(d) Average current error in a switching cycle

Figure 3.5 Simulated waveforms under the nominal condition



(a) Current error in a switching cycle (b) Average current error in a switching cycle

Figure 3.6 Simulated waveforms with higher switching frequency

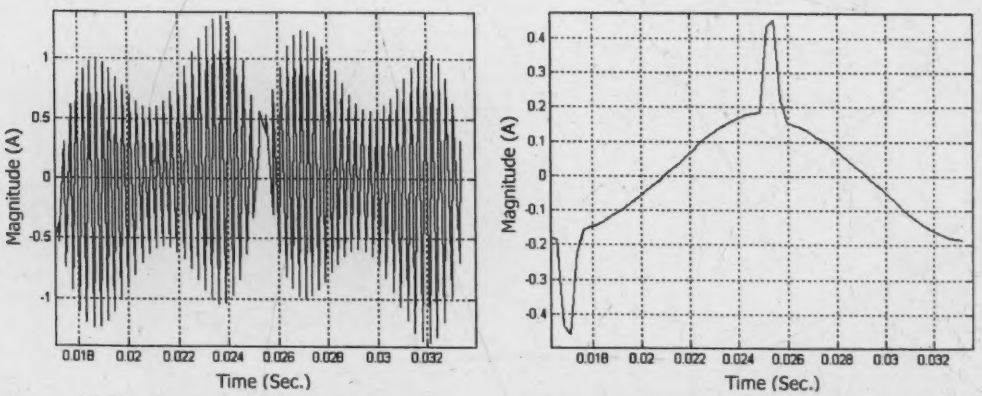
The determination on the zero crossing of the modulated voltage source V_i in Fig. 1.2 is based upon the zero crossing of the supply voltage for this scheme. However, the existence of the two apparent deviations in the current error waveform in this case is less satisfying, as shown in Fig. 3.5 (d). Simulation waveforms in Fig. 3.6 present the current error and the average current error with the same simulation condition as in the nominal case except that the switching frequency is set at 3KHz. It is quite obvious that the deviations caused by the zero crossing are severe in this case.

The supply current is lagging of the supply voltage due to the supply inductor in the circuit. Hence the determination of the zero crossing of the modulated voltage source should not be on the basis of the zero crossing of the supply voltage. An improvement about this issue is expected for the practical applications. These apparent deviations could be attenuated by more sophisticated control algorithm or simply, connecting a small resistor in series with the inductor to mitigate the spikes.

3.4.2 Simulation Under the Emulated Practical Condition

Model-based predictive current control scheme is sensitive to the circuit parameters variations. This is because all the model parameters are involved directly to predict the suitable

switching instant. It produces less satisfactory performance if any of the mismatches exist between the real circuit and the assumed circuit model, such as the inductance mismatch. It also happens when the practical work condition drifts away from the assumed ideal situation, such as the existence of the second harmonic in the dc link voltage and the noise in the ac supply voltage. The non-zero average current error and hence certain amount of low order harmonics are inevitable in theses cases. For the following examinations, only the parameters other than those in the nominal simulation condition, as listed in Table 3.1, are listed out separately.



(a) Supply current in a switching cycle (b) Average current error in a switching cycle

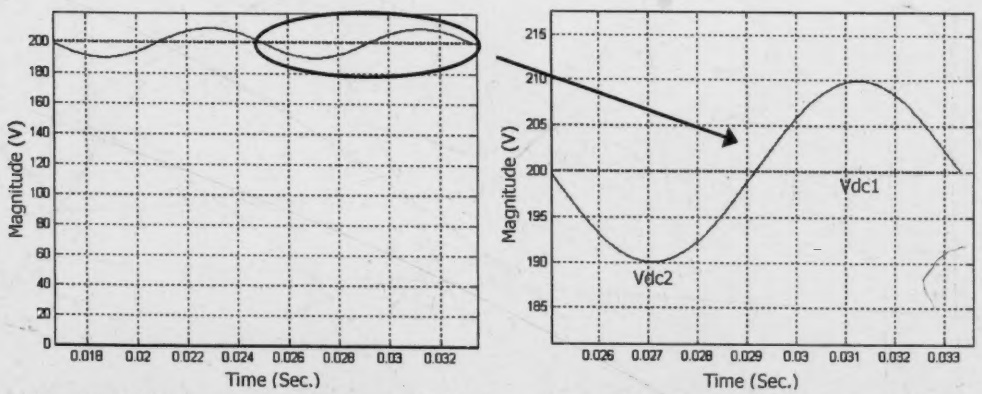
Figure 3.7 Simulated waveforms with 20% supply inductance mismatch

Table 3.2 Different circuit parameters of simulation waveforms in Fig. 3.7

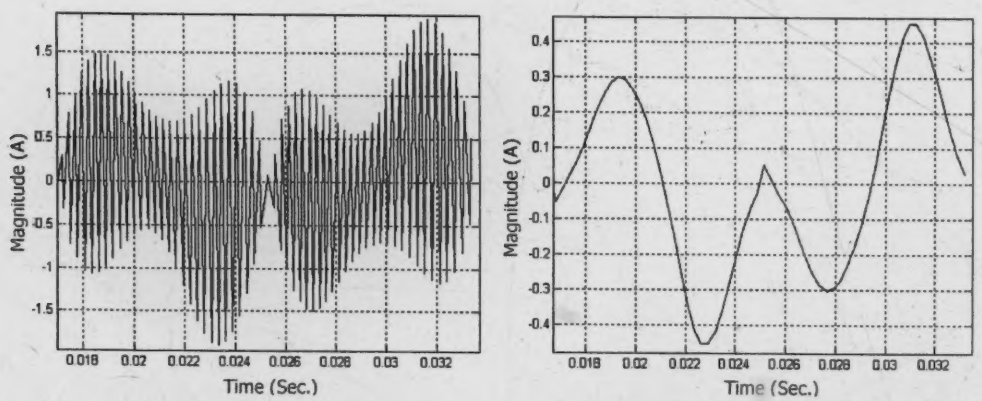
Parameters	Circuit Values	Model Values
Supply Inductance (L)	*5mH*	*6mH*

The first examination is to investigate the effectiveness of the control algorithm with the existence of the mismatch between the circuit parameters and the model parameters. The 20% mismatch of the inductance between the circuit value and the model value, as listed in Table 3.2, gives rise to around 12% maximum excursion of the average current error deviate away from the zero line, as shown in Fig. 3.7 (b). Moreover, the apparent deviations caused by the zero crossing of the supply voltage present longer lasting and higher amplitudes under this condition.

Likewise, the existence of the second harmonic in the dc link voltage, as listed in Table 3.3, produces the apparent excursions of the average current error, as shown in Fig. 3.8. The irregular shape of the average current error reveals the existence of the low order harmonics of the supply current. The 5% maximum variation of the dc link voltage brings in around 30% maximum deviation of the average current error away from the zero line.



(a) Nominal 200V dc voltage and the one with 5% second harmonic variances (b) Expanded scale

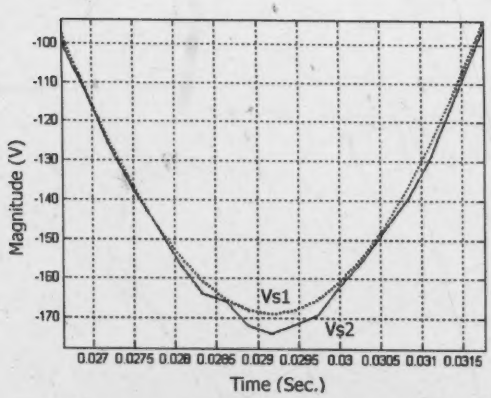


(c) Current error in a switching cycle (d) Average current error in a switching cycle

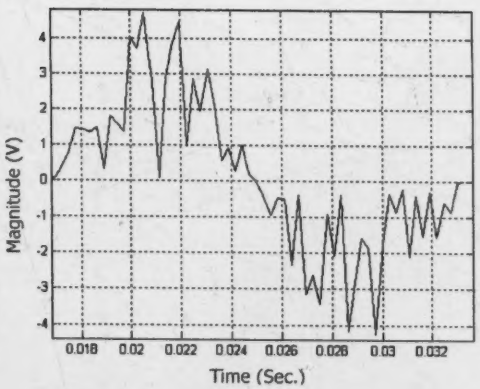
Figure 3.8 Waveforms with the injected 5% second harmonic in dc link voltage

Table 3.3 Different circuit parameters of simulation waveforms in Fig. 3.8

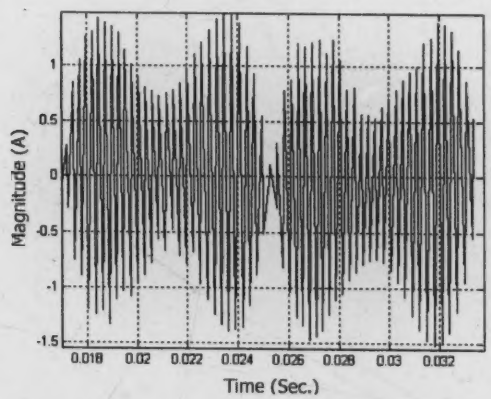
Parameters	Circuit Values	Model Values
dc Link Voltage (E)	V_{dc1}: *200V*	V_{dc2}: *200-10*sin240πt V*



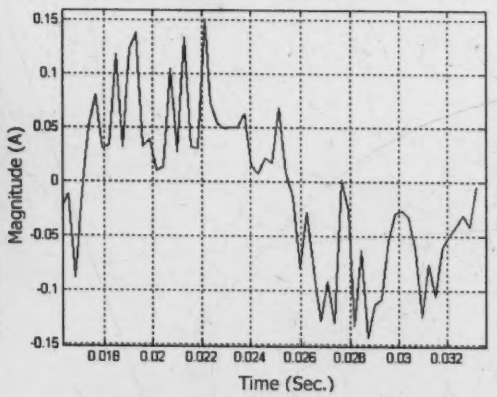
(a) Ideal supply voltage and the one with 3% maximum random noise



(b) Injected random noise



(c) Current error in a switching cycle



(d) Average current error in a switching cycle

Figure 3.9 Waveforms with random noise in supply voltage

Table 3.4 Different circuit parameters of simulation waveforms in Fig. 3.9

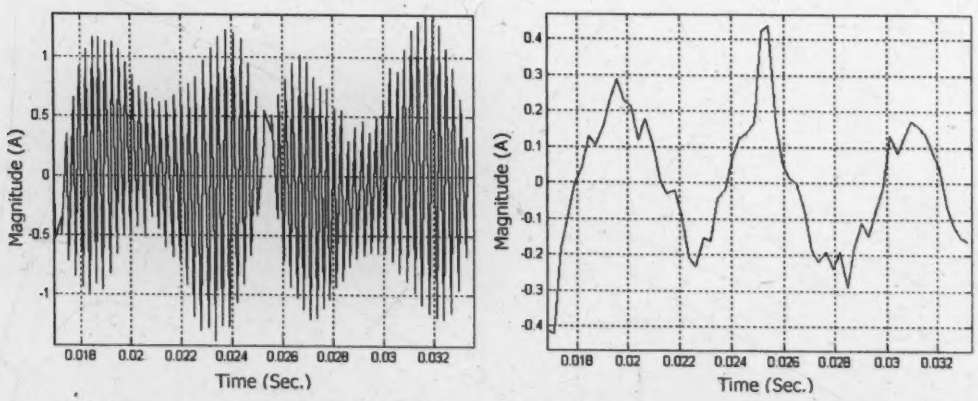
Parameters	Circuit Values	Model Values
Supply Voltage (V_{pk})	V_{s1}: *169V, 60Hz*	V_{s2}: *169+5*rand*① *V, 60Hz*

Note ①: *rand* designates the random noise with the maximum amplitude of 1V

The noise rejection capability of the proposed control scheme is slightly less than expected, as shown in Fig. 3.9. The 3% maximum variations of the noise of the ac supply voltage, as listed in table 3.4, produces not only the noise contents but also around 10% maximum deviation of the average current error away from the zero line. The abnormal shape of the

average current error exhibits the existence of the noise in the circuit. Since noise is unavoidable in the practical experimental environment, control strategies with bigger noise margin are desired for the practical application.

The waveforms of the proposed current control scheme are presented in Fig. 3.10, with the combined cases of 20% inductance impedance mismatch between the circuit value and the model value, 5% second harmonic in dc link voltage and 3% noise in ac supply voltage, as listed in Table 3.5.



(a) Current error in a switching cycle (b) Average current error in a switching cycle

Figure 3.10 Waveforms with 5% second harmonic, 3% random noise, 20% inductance mismatch

Table 3.5 Circuit parameters of simulation waveforms in Fig. 3.10

Parameters	Circuit Values	Model Values
Supply Inductance (L)	*5mH*	*6mH*
Supply Voltage (V_{pk})	*169V, 60Hz*	*169+5*randV, 60Hz*
dc Link Voltage (E)	*200V*	*200-10*sin240πt V*
Switching Frequency (f_{sw})	1800Hz	Not required
Clock Frequency	3600Hz	Not required
Current Reference (I_{ref})	10A	Not required

The average current error under this simulation condition presents around 30% maximum deviation of the average current away from the zero line. Though the resultant waveform of the average current error is not the linear combination of the waveforms in the three separate cases, it still displays the obvious features of every case, such as the apparent deviations due to the zero crossing of the supply voltage, and the irregular shape of the average current error due to the existence of the noise. It is apparent that the intended control goal, the symmetrical zero-centered current error, is not quite accomplished. In this sense, this control scheme is sensitive to the circuit parameters variations.

3.5 Summary

Model-based predictive current control has been introduced in this chapter. This scheme determines the intended switching instants merely based upon the pre-defined model values without any current feedback included. The resultant current control scheme is sensitive to the circuit parameters variations. A symmetrical zero-centered current error is obtained provided the real-time measured actual parameters match the pre-established circuit model values.

As discussed in section 3.3, this scheme is simulated in MATLAB program using a conceptual comparator. This also implies that this scheme has a potential to be implemented using specially designed analogue circuits that could realize multiple and sine, cosine functions. However, a further investigation about this scheme is required to bring to fruition a current feedback loop and to improve the performance of the scheme in the practical environment.

The proposed scheme is not suitable for DSP implementation since no direct solution has been developed for real-time computation. However, the basic concepts and the relevant equations of this scheme form the basic for a new slope detective control scheme that is described in Chapter 4. This second scheme gives a direct solution that is suitable for DSP implementation and has an improved performance in terms of strong capability against circuit parameters variations, high noise and harmonics rejection capability, stable and fairly fast transient response.

Chapter 4 Slope Detective Current Control

Motivated by the basic control concepts derived for model-based predictive current control, see chapter 3, a control scheme that is suitable for practical applications is proposed in this chapter. Slope detective current control is a digital-based constant switching frequency unipolar PWM control algorithm that successfully regulates the inductor current of a PWM rectifier to precisely follow the pre-established current reference signal. This is accomplished by choosing the desired switching instant so as to achieve a symmetrical zero-centered supply current ripple in every switching period.

Slope detective current control uses the slopes of the current error signal in the previous two successive switching cycles to determine when the next switching instant should occur. Unlike model-based predictive current control, the desired switching instant is chosen based upon the real-time measurements of the actual parameters rather than circuit model parameters. As a result, a feedback loop for the supply current signal is essential for this control scheme.

Intuitive descriptions and the basic concepts of slope detective current control scheme are introduced in this chapter. In addition, the relevant formulas that lead to quantitative analysis are also presented. Simulated characteristics for the single-phase PWM rectifier topology are used to compare the performance of the proposed control scheme with those of other control schemes, such as ramp comparison current control, fix band hysteresis current control, and variable band hysteresis current control scheme.

4.1 General Description

The basic control concept of ***slope detective current control scheme*** is explained based upon the single-phase PWM rectifier bridge topology, as illustrated in the block diagram in Fig. 4.1. Unlike model-based predictive current control, determination of the intended switching instant of the proposed control scheme depends upon the real-time measurement of the actual parameters. This is accomplished by using the real-time sampled slopes of the current error

signal as an input to the controller. The current error signal, a difference between the sampled supply current and the current reference, contains not only the information of circuit parameters, but also a trend in the natural of signal change over time. In other words, the change of the current error signal from cycle to cycle is to produce what the likely shape of the current error signal in the upcoming cycle. To simplify the analysis procedure, the dc link is treated as a well regulated constant dc voltage and the semiconductor switches are regarded as ideal switches regardless of the real device physical characteristics.

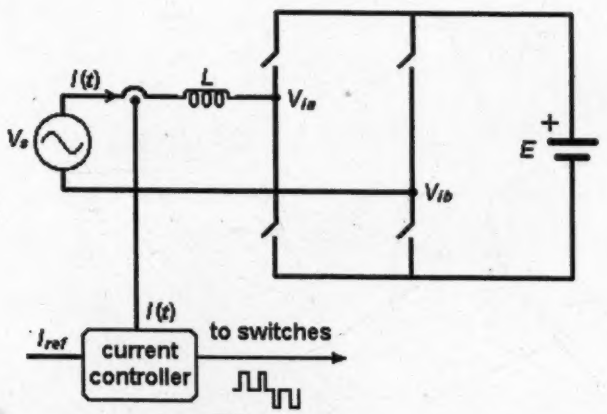


Figure 4.1 Block diagram of slope detective current control scheme

The control algorithm applied to the single-phase PWM rectifier bridge is intended to achieve a symmetrical zero-centered current error signal. To obtain the control goal, the current error signal must vary in two opposite directions around zero in every PWM switching cycle. Therefore, the current error signal always has two distinct varying segments within each switching period, the ramping upward segment and the ramping downward segment, as shown in Fig. 4.2. As discussed in Chapter 3, the current error signal of the two segments can be expressed in terms of the circuit parameters, referring to Eq. (3.13) and Eq. (3.16), according to the circuit model shown in Fig. 1.2.

Generally, the current error signal is assumed to ramp linearly provided the switching frequency is high enough. The assumption of the linear varying current error signal introduces

two distinct and constant slopes of the current error signal within a switching period. The value of each slope is determined by taking the real-time measurements of the two instantaneous magnitudes, the maximum and the minimum magnitudes of the current error signal.

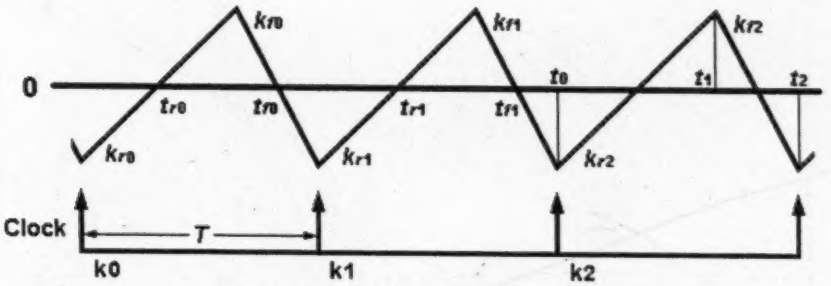


Figure 4.2 Principle of slope detective current control

On the other hand, since two segments of the current error signal can be described with equations using the circuit parameters, the slopes of the current error signal can also be defined with equations. By applying the small signal assumption, Taylor expansion theorem and basic trigonometric function transformations can be used to theoretically simplify the expressions for the slopes of the current error signal. Consequently, two distinct and constant slopes in each switching period are approximated as the coefficients of the first-degree terms of the Taylor polynomials, depending on the different expressions of two segments respectively.

The goal of the simplification is to eliminate all the involving circuit parameters for determination of the suitable switching instant and to replace them by the dynamically sampled actual parameters. However, the slopes, expressed as the coefficients of the first-degree terms of the Taylor polynomials, still contain the undesirable circuit parameters. By manipulating the relevant equations, the ramping up and ramping down slopes k_{r2} and k_{f2}, as shown in Fig. 4.2, can be expressed by the slopes k_{r0}, k_{r1}, k_{f0}, k_{f1} in the previous two successive switching cycles, without any circuit parameters involved in.

According to the discussion in Chapter 3, the time instants t_0 and t_2 are always known for the proposed algorithm since they are fixed points once the switching frequency is determined.

The slope k_{r2}, on the other hand, is also a slope of the line function between the two time instants t_0 and t_1. The slope k_{f2}, similar as k_{r2}, can also be expressed by the magnitudes and time values of the two time instants t_1 and t_2. With the control law to obtain a symmetrical zero-centered inductor current ripple whose peaks occur at the time instant t_1 and t_2 respectively in every PWM switching cycle, the only unknown switching instant t_1 can be solved and expressed by all known variables, such as t_0, t_2, k_{r0}, k_{r1}, k_{f0}, k_{f1}, etc. In this sense, the choice of the intended switching instant t_1 is not based upon the circuit parameters, but related with the real-time measurements of the actual parameters.

The proposed control scheme is based upon digital techniques. The constant switching frequency is guaranteed by the fixed digital clock rate, rather than the triangular carrier reference. It is the quick advanced digital technology that makes the real-time cycle-to-cycle calculation for the desired switching instant become possible. Consequently, accurate control over the ac supply current is accomplished.

The proposed control scheme is a fixed switching frequency scheme that achieves a symmetrical zero-centered current error in every PWM switching cycle. It provides accurate control over the supply current signal, oscillating within symmetrical bands centered on the current reference. The control scheme presents unity PF performance that could be accomplished under a relatively low switching frequency, indicating low switching losses and high efficiency. These features make the proposed control scheme very suitable for high power and accurate control applications.

The proposed control scheme has high performance in terms of accurate control of the ac supply current, high immunity over circuit parameters variations, stable and fairly fast transient response, and extremely narrow switching frequency band. The employed unipolar PWM scheme introduces low supply current ripple that brings the benefits of a small supply inductor or a low switching frequency. It also have the effect to push the high order harmonics into high frequency band so that the harmonics can be filtered away very easily. All the merits of the proposed scheme are clarified by the simulated characteristics in section 4.4 and the comparison

with other current control schemes in section 4.5.

The proposed control scheme produces better performance under the higher switching frequency. This is ascribed to the small signal approximation applied to the scheme. The zero crossing issue, a common problem due to unipolar PWM scheme [4,20], is significantly mitigated in this control scheme and is discussed in detail in section 4.3. However, due to the prediction of the intended switching instant being based upon the slopes in the previous switching period, the quality of the current waveshaping deteriorates at the crest points of the supply voltage within the line cycle. This is attributed to the slope of the supply voltage changing the polarity around the two crest points, referring to Eq. (4.32), Eq. (4.44) and Fig. 4.6 (d). Higher switching frequency is required to reduce the effect of this issue and to produce better performance.

4.2 Formula Derivation

The general description of the proposed algorithm in section 4.1 is intended to give an overview of the proposed scheme. In this section, the detailed formula derivations and relevant background mathematic knowledge are stated. Before any detailed analysis begins, the concept of the small signal approximation is illustrated again, for all the simplification applied to the formulas is based upon it.

The relatively high switching frequency f_{sw}, with respect to the modulated line frequency, intercepts a long and slow varying sinusoidal period into a number of short time intervals, namely switching periods, depending on the ratio between the switching frequency and the modulated line frequency. In each short switching period, it is reasonable to assume that the slow varying modulated sinusoidal signal is invariable with time, provided the switching frequency is high enough. The resulted small signal range produces the possibility to simplify the nonlinear characterises of the bridge operation to be linear. The linearization for the relevant formulas of the proposed scheme is mainly based upon Taylor polynomials theorem and trigonometric functions transformations, which are attached in Appendix F.

4.2.1 Two Approaches to Describe the Slopes of the Current Error Signal

A sketch of the current error signal in one PWM switching cycle in Fig. 4.3 is used to explain the proposed control scheme applied on the single-phase PWM rectifier. It is obvious that the current error has two distinct and constant slopes over a PWM switching cycle. The time instant t_r is the zero crossing during the process of its first ramping segment, while the time instant t_f is the other zero crossing during the process of its second ramping segment, as shown in Fig. 4.3.

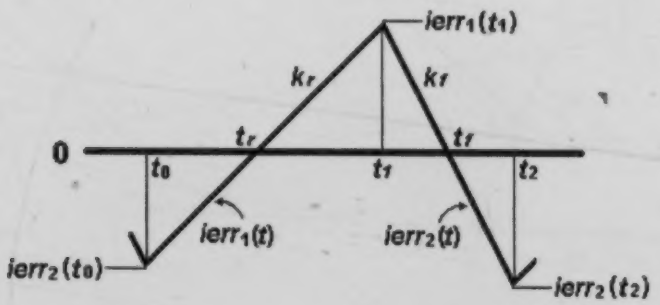


Figure 4.3 Current error waveform with fixed frequency clock

The formula of the current error signal for its first ramping segment term $ierr_1(t)$ in Eq. (3.13), has the first-degree Taylor polynomials at the zero crossing time instant t_r as follows:

$$ierr_1(t) = ierr_1(t_r) + \frac{ierr_1^{(1)}(t_r)}{1!}(t - t_r) + R_1(t) \tag{4.1}$$

In which, the first constant term of the function $ierr_1(t)$ has its value equal to zero at the zero crossing time instant t_r. The coefficient of the differential term of the function $ierr_1(t)$ at the time instant t_r is designated as k_r in Eq. (4.2). This coefficient k_r is interpreted as the approximate slope of the current error signal during the first ramping process as long as the remainder term, the rest of the high order polynomials of the Taylor expansion, are small enough to be ignored. Therefore,

$$k_r = ierr_1^{(1)}(t_r) = \frac{V_{pk}}{L}\sin\omega t_r - \omega I_{pk}\cos\omega t_r \tag{4.2}$$

Substituting Eq. (4.2) back into Eq. (4.1), yields the linearized current error $ierr_1(t)$ as,

$$ierr_1(t) = \left(\frac{V_{pk}}{L} \sin \omega t_r - \omega I_{pk} \cos \omega t_r \right) \cdot (t - t_r) \tag{4.3}$$

On the other hand, the real current error can be obtained by the real-time sensoring on the magnitude of the current error signal. With the corresponding time instants, the slopes of the current error signal can be approximated in a manner of linear equations. Accordingly, the slope k_r of the current error signal $ierr_1(t)$ has another way to be given as,

$$k_r = \frac{ierr_1(t_1) - ierr_2(t_0)}{t_1 - t_0} \tag{4.4}$$

For the second ramping process, the time instant t_f is the zero crossing of the current error signal $ierr_2(t)$, as shown in Fig. 4.3. Due to the similar nature of the two significant time instants t_r and t_f, all the foregoing theorems and assumptions developed for the time instant t_r are also applicable to the other time instant t_f. For the second ramping process of the current error signal, the corresponding approximate slope, namely the coefficient of the differential term of the function $ierr_2(t)$ is designated as k_f.

It is worth to point out that the two slopes k_r and k_f always have opposite signs. This requirement has its reasonable explanation that the controlled current always oscillates around the pre-established current reference. In other words, the current error ramps in one direction during the first ramping process, it ramps in the opposite direction during the second ramping process. The current is allowed to merely vary around the zero error line to minimize the average current error and hence the low order harmonics.

Likewise, the relevant formulas for the second ramping process about the current error signal $ierr_2(t)$ and its corresponding slope k_f are given as follows:

$$k_f = ierr_2^{(1)}(t_f) = \frac{V_{pk}}{L} \sin \omega t_f - \omega I_{pk} \cos \omega t_f - sign(V_s) \cdot \frac{E}{L} \tag{4.5}$$

$$ierr_2(t) = \left(\frac{V_{pk}}{L} \sin \omega t_f - \omega I_{pk} \cos \omega t_f - sign(V_s) \cdot \frac{E}{L} \right) \cdot (t - t_f) \tag{4.6}$$

$$k_f = \frac{ierr_2(t_2) - ierr_1(t_1)}{t_2 - t_1} \tag{4.7}$$

4.2.2 Prediction on the Slope —the First Ramping Process

Since the slope of the current error signal can be described from two different view points, circuit equations and sampled data, efforts are put on seeking a proper way to express the unknown slope k_{r2} and k_{f2} by the known slopes k_{r1}, k_{f1}, k_{r0}, and k_{f0} in the previous two successive switching periods k1 and k0, as shown in Fig. 4.2. If such expressions would be found then the suitable switching instant for switching period k2 could be predicted without any knowledge of the parameters of the circuit model, which leads to the non-zero average current error under the conditions of the parameters variations and noise perturbations.

t_{r0} and t_{r1}, as shown in Fig. 4.2, are the zero crossing time instants of the first ramping segments in the first two switching cycles k0 and k1, among the three successive switching periods. Hence, k_{r0} and k_{r1} could be given in terms of t_{r0} and t_{r1} according to Eq. (4.2), respectively,

$$k_{r0} = \frac{V_{pk}}{L}\sin\omega t_{r0} - \omega I_{pk}\cos\omega t_{r0} \tag{4.8}$$

$$k_{r1} = \frac{V_{pk}}{L}\sin\omega t_{r1} - \omega I_{pk}\cos\omega t_{r1} \tag{4.9}$$

The time difference between time instants t_{r0} and t_{r1} is not exactly the same as the switching time period. However, for the two successive switching periods, it is reasonable to make the assumption that the time difference between t_{r0} and t_{r1} is the switching time period T, for the error comes up with the assumption is negligible. Rewriting Eq. (4.9) accordingly,

$$k_{r1} \approx \frac{V_{pk}}{L}\sin\omega(t_{r0} + T) - \omega I_{pk}\cos\omega(t_{r0} + T) \tag{4.10}$$

For bipolar PWM scheme, the switching time period T is just the reciprocal of the switching frequency f_{sw}. However, unipolar PWM scheme presents the "double frequency"

effect as one of its benefits. Hence in this case the switching time period T is obtained as,

$$T = \frac{1}{2f_{sw}} \tag{4.11}$$

Subtracting k_{r0} in Eq. (4.8) from k_{r1} in Eq. (4.10) and rearranging it yields,

$$k_{r1} - k_{r0} = \frac{V_{pk}}{L}\left(\sin\omega\left(t_{r0}+T\right) - \sin\omega t_{r0}\right) - \omega I_{pk}\left(\cos\omega\left(t_{r0}+T\right) - \cos\omega t_{r0}\right) \tag{4.12}$$

The above equation could be further simplified according to the trigonometric functions in Eq. (F.2) and (F.3),

$$k_{r1} - k_{r0} = \sin\frac{\omega T}{2}\left(2\frac{V_{pk}}{L}\cos\omega\left(t_{r0}+\frac{T}{2}\right) + 2\omega I_{pk}\sin\omega\left(t_{r0}+\frac{T}{2}\right)\right) \tag{4.13}$$

In the above equation, the product term outside the bracket is a constant number as long as the switching frequency has been determined. Generally, the switching frequency is relatively high with respect to the line frequency. As a result, the term $\omega T/2$ is always a very small value close to zero. Hence it can be further linearized according to Eq. (F.7),

$$\sin\frac{\omega T}{2} = \frac{\omega T}{2} \tag{4.14}$$

Substituting Eq. (4.14) into Eq. (4.13) and rearranging it gives,

$$k_{r1} - k_{r0} = \omega T \cdot \left(\frac{V_{pk}}{L}\cos\omega\left(t_{r0}+\frac{T}{2}\right) + \omega I_{pk}\sin\omega\left(t_{r0}+\frac{T}{2}\right)\right) \tag{4.15}$$

Dividing the term ωT on both sides of Eq. (4.15) yields,

$$\frac{k_{r1} - k_{r0}}{\omega T} = \frac{V_{pk}}{L}\cos\omega\left(t_{r0}+\frac{T}{2}\right) + \omega I_{pk}\sin\omega\left(t_{r0}+\frac{T}{2}\right) \tag{4.16}$$

The two terms on the right hand side of the above equation are not straight forward and do not provide any meaningful and simplified results as given. In the above equation, all the circuit parameters, sine and cosine terms are involved, indicating less satisfactory performance (refer to section 3.4) and computational complexity. Further simplification can be undertaken to eliminate the involvement of the circuit parameters, sine and cosine terms. The two terms in Eq. (4.16) are analyzed separately. According to the trigonometric functions in Eq. (F.4), the cosine

term on the right hand of Eq. (4.16) is derived as,

$$\cos\omega\left(t_{r0}+\frac{T}{2}\right)=\cos\omega t_{r0}\cos\frac{\omega T}{2}-\sin\omega t_{r0}\sin\frac{\omega T}{2} \tag{4.17}$$

The second term on the right hand of the above equation requires the simplified result given in Eq. (4.14). Its cosine term in Eq (4.17) can also be simplified according to Eq. (F.8) for the same reason and is given in Eq. (4.18).

$$\cos\frac{\omega T}{2}=1-\frac{(\omega T)^2}{2} \tag{4.18}$$

The second term on the right hand in the above equation is so small that it could be neglected in this case, bringing no significant impact on the accuracy of the control goal. For example, under the condition of an 1.8KHz switching frequency for unipolar PWM and a 60Hz line frequency, the two involved terms ω and T have the values as *376.99 rad/s*$^{-1}$ and *277.77 μs* respectively. Consequently, the value of the second item in the above equation is obtained as *0.00548 rad*^{2}, a very small fraction. Moreover, neglecting the second term on the right hand in the above equation could avoid the unnecessary complicated inter-process during the simplification procedure that provides no further performance improvements. In this sense, the final simplification result for the cosine function is:

$$\cos\frac{\omega T}{2}\approx 1 \tag{4.19}$$

Substituting the simplified Eq. (4.14) and Eq. (4.19) into Eq. (4.17) gives:

$$\cos\omega\left(t_{r0}+\frac{T}{2}\right)=\cos\omega t_{r0}-\frac{\omega T}{2}\sin\omega t_{r0} \tag{4.20}$$

Following the derivation process of the first term on the right hand of Eq. (4.16), the second term on the right hand of Eq. (4.16) is derived according to the trigonometric functions in Eq. (F.5),

$$\sin\omega\left(t_{r0}+\frac{T}{2}\right)=\sin\omega t_{r0}\cos\frac{\omega T}{2}+\cos\omega t_{r0}\sin\frac{\omega T}{2} \tag{4.21}$$

Substituting the simplified Eq. (4.14) and Eq. (4.19) in the above equation yields,

$$\sin\omega\left(t_{r0}+\frac{T}{2}\right)=\sin\omega t_{r0}+\frac{\omega T}{2}\cos\omega t_{r0} \tag{4.22}$$

Substituting Eq. (4.20) and Eq. (4.22) into Eq. (4.16), and rearranging it gives,

$$\frac{k_{r1}-k_{r0}}{\omega T}=\frac{V_{pk}}{L}\cos\omega t_{r0}+\omega I_{pk}\sin\omega t_{r0}-\frac{\omega T}{2}\left(\frac{V_{pk}}{L}\sin\omega t_{r0}-\omega I_{pk}\cos\omega t_{r0}\right) \tag{4.23}$$

The expression in the bracket of the above equation is actually the equation to describe k_{r0}, see Eq. (4.8). Substituting k_{r0} into Eq. (4.23) and rearranging it gives,

$$\frac{k_{r1}-k_{r0}}{\omega T}+\frac{\omega T}{2}k_{r0}=\frac{V_{pk}}{L}\cos\omega t_{r0}+\omega I_{pk}\sin\omega t_{r0} \tag{4.24}$$

Squaring both sides of the above equation yields,

$$\left(\frac{k_{r1}-k_{r0}}{\omega T}+\frac{\omega T}{2}k_{r0}\right)^2=\left(\frac{V_{pk}}{L}\cos\omega t_{r0}\right)^2+\left(\omega I_{pk}\sin\omega t_{r0}\right)^2 +2\frac{\omega V_{pk}I_{pk}}{L}\cos\omega t_{r0}\sin\omega t_{r0} \tag{4.25}$$

Squaring both sides of Eq. (4.8) gives,

$$k_{r0}{}^2=\left(\frac{V_{pk}}{L}\sin\omega t_{r0}\right)^2+\left(\omega I_{pk}\cos\omega t_{r0}\right)^2-2\frac{\omega V_{pk}I_{pk}}{L}\cos\omega t_{r0}\sin\omega t_{r0} \tag{4.26}$$

Adding together Eq. (4.25) and Eq. (4.26), simplifying according to the trigonometric functions in Eq. (F.1) and rearranging it yields,

$$\left(\frac{k_{r1}-k_{r0}}{\omega T}+\frac{\omega T}{2}k_{r0}\right)^2+k_{r0}{}^2=\left(\frac{V_{pk}}{L}\right)^2+\left(\omega I_{pk}\right)^2 \tag{4.27}$$

The main purpose of all these linear simplifications is to eliminate all the involving circuit parameters, such as V_{pk}, I_{pk}, L, and E. Although these undesirable parameters are still included in Eq. (4.27), they display in Eq. (4.27) as a form of constants, without involving any sine and cosine terms. Therefore, if three switching cycles are picked, these constants can be eliminated.

For the second and the third switching period k1 and k2, as shown in Fig. 4.2, the formula links the corresponding slopes k_{r1} and k_{r2} are obtained in the same form according to Eq. (4.27),

$$\left(\frac{k_{r2}-k_{r1}}{\omega T}+\frac{\omega T}{2}k_{r1}\right)^2+k_{r1}^{\ 2}=\left(\frac{V_{pk}}{L}\right)^2+\left(\omega I_{pk}\right)^2 \tag{4.28}$$

Subtracting Eq. (4.27) from Eq. (4.28) and rearranging it gives,

$$\left(\frac{k_{r2}-k_{r1}}{\omega T}+\frac{\omega T}{2}k_{r1}\right)^2=\left(\frac{k_{r1}-k_{r0}}{\omega T}+\frac{\omega T}{2}k_{r0}\right)^2-\left(k_{r1}^{\ 2}-k_{r0}^{\ 2}\right) \tag{4.29}$$

In Eq. (4.29), k_{r1} and k_{r0} are the ramping slopes that can be obtained by sampling and calculating over the real current errors and the corresponding time instants. Hence all the information about the real circuit functioning is contained in the two detected ramping slopes. The ramping slope k_{r2} is the one that can be predicted from the ramping slopes k_{r1} and k_{r0} in the previous two successive switching periods k0 and k1, according to Eq. (4.29). It is obvious that no circuit parameters are involved in the prediction of the ramping slope k_{r2} for the switching cycle k2.

It is a desirable feature for slope detective current control scheme that no knowledge of the circuit parameters is required to predict the desired switching instant, referring to Eq. (4.29). The proposed control scheme works independently from the changes in circuit parameters and has high immunity of noise perturbations. The proposed control scheme is more suitable for practical application with respect to model-based predictive control scheme discussed in Chapter 3.

An expression for the predicted ramping slope k_{r2} is derived as follows:

$$\frac{k_{r2}-k_{r1}}{\omega T}=\pm\sqrt{\left(\frac{k_{r1}-k_{r0}}{\omega T}+\frac{\omega T}{2}k_{r0}\right)^2-\left(k_{r1}^{\ 2}-k_{r0}^{\ 2}\right)}-\frac{\omega T}{2}k_{r1} \tag{4.30}$$

Hence,

$$k_{r2}=k_{r1}-\frac{(\omega T)^2}{2}k_{r1}\pm\sqrt{\left(k_{r1}-k_{r0}+\frac{(\omega T)^2}{2}k_{r0}\right)^2-(\omega T)^2\cdot\left(k_{r1}^{\ 2}-k_{r0}^{\ 2}\right)} \tag{4.31}$$

The trend in changes between slopes k_{r1} and k_{r0} is closely related to the trend-of-rate of the ac supply voltage. In the two successive switching cycles, the rate-of-change over the magnitude of the supply voltage is much faster than the rate-of-change over the magnitude of

the dc link voltage. In this sense, the dc link voltage could be treated as a constant with respect to the relatively rapid rate-of-change of the supply voltage.

In the single-phase PWM rectifier bridge circuit model shown in Fig. 1.2, the voltage difference between the supply voltage V_s and the modulated voltage V_i is carried by the induced voltage across the inductor V_L. The modulated voltage signal V_i always has two states, for example E and 0 as shown in Fig. 4.4, during one PWM switching cycle. Due to the reason stated in the previous paragraph, these two states are of relatively slow rate-of-change on the magnitude with respect to the rate-of-change of the magnitude of the supply voltage V_s. On the other hand, the induced voltage across the inductor is proportional to the rate-of-change of the current through the inductor. As a result, the rate-of-change of the controlled ac supply current is primarily dependent on the rate-of-change of the supply voltage.

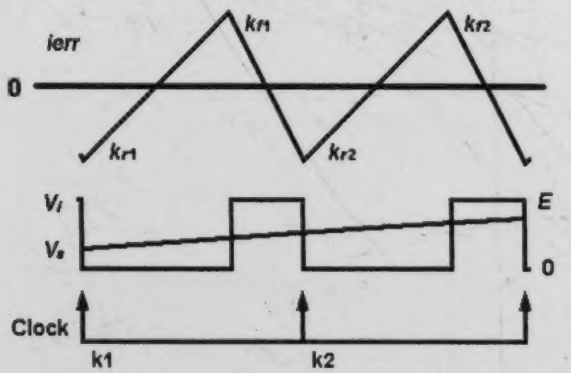


Figure 4.4 Current error, supply voltage and dc link voltage waveforms

Although the slope of the current error is not the same as the slope of the supply current, it follows the same trend in changes as the rate-of-change of the supply current. For instance, the slope of the current error k_{r2} is bigger than the slope of the current error k_{r1} because the supply voltage V_s in switching cycle k2 is higher than it in switching cycle k1, as shown in Fig. 4.4. The higher the supply voltage is, the steeper the slope of the current error it has.

Due to the foregoing discussions, the rate-of-change of the supply voltage determines the trend in changes of the slope of the current error. Since the supply voltage has its form as a

sinusoidal function the rate-of-change of it is in the form of a cosine function. In Eq. (4.31) the trend in changes of the slope k_{r2} is primarily determined by the third term because the second term is very small as discussed before. In light of this, Eq. (4.31) can be rewritten so that the plus and minus sign in the equation is replaced and more clearly stated as,

$$k_{r2} = k_{r1} + sign(\cos\omega t)\cdot\sqrt{(k_{r1}-k_{r0})^2 - (\omega T)^2\cdot(k_{r1}^{\ 2} - k_{r0}^{\ 2})} \qquad (4.32)$$

Where, *sign* designates a function to get the relevant sign with the value of +1, -1 , or 0 for the cosine function value in the bracket.

4.2.3 Prediction on the Slope ---the Second Ramping Process

The current error slope of the first ramping segment in switching period k2 can be expressed by the slopes of the previous two successive periods k1 and k0, as discussed in section 4.2.2. In the similar way, the current error slope of the second ramping process can be derived and expressed by all the known slopes k_{r1}, k_{r0}, k_{f1}, and k_{f0} in the two successive switching periods k1 and k0.

t_{f0} and t_{f1} are the zero crossing points in the second ramping segments of the first two switching cycles k0 and k1 among the three successive switching periods, as shown in Fig. 4.2. Hence, k_{f0} and k_{f1} can be given in terms of t_{f0} and t_{f1} according to Eq. (4.5), respectively,

$$k_{f0} = \frac{V_{pk}}{L}\sin\omega t_{f0} - \omega I_{pk}\cos\omega t_{f0} - sign(V_s)\cdot\frac{E}{L} \qquad (4.33)$$

$$k_{f1} = \frac{V_{pk}}{L}\sin\omega t_{f1} - \omega I_{pk}\cos\omega t_{f1} - sign(V_s)\cdot\frac{E}{L} \qquad (4.34)$$

Due to the similar reason discussed before, assuming the time difference between time instant t_{f0} and t_{f1} is equal to the switching time period T, therefore,

$$k_{f1} \approx \frac{V_{pk}}{L}\sin\omega(t_{f0}+T) - \omega I_{pk}\cos\omega(t_{f0}+T) - sign(V_s)\cdot\frac{E}{L} \qquad (4.35)$$

Subtracting k_{f0} in Eq. (4.33) from k_{f1} in Eq. (4.35) and following the similar simplifying procedures gives,

$$k_{f1} - k_{f0} = \omega T \cdot \left(\frac{V_{pk}}{L} \cos \omega \left(t_{f0} + \frac{T}{2} \right) + \omega I_{pk} \sin \omega \left(t_{f0} + \frac{T}{2} \right) \right) \tag{4.36}$$

The time difference between time instants t_{f0} and t_{r1} is approximated to be $T/2$. The error comes up with the assumption is negligible provided the switching frequency is high enough. Hence,

$$\sin \omega (t_{r0} + T) \approx \sin \omega \left(t_{f0} + \frac{T}{2} \right) \quad \& \quad \cos \omega (t_{r0} + T) \approx \cos \omega \left(t_{f0} + \frac{T}{2} \right)$$

Substituting the above assumption into Eq. (4.36) yields,

$$k_{f1} - k_{f0} = \omega T \cdot \left(\frac{V_{pk}}{L} \cos \omega (t_{r0} + T) + \omega I_{pk} \sin \omega (t_{r0} + T) \right) \tag{4.37}$$

Dividing the term ωT on both sides of Eq. (4.37) yields,

$$\frac{k_{f1} - k_{f0}}{\omega T} = \frac{V_{pk}}{L} \cos \omega (t_{r0} + T) + \omega I_{pk} \sin \omega (t_{r0} + T) \tag{4.38}$$

Squaring both sides of Eq. (4.38) and Eq. (4.10), adding the squared two equations together gives,

$$\left(\frac{k_{f1} - k_{f0}}{\omega T} \right)^2 + (k_{r1})^2 = \left(\frac{V_{pk}}{L} \right)^2 + (\omega I_{pk})^2 \tag{4.39}$$

Due to the same reason as mentioned before, the circuit parameters are still involved on the right side of Eq. (4.39). As a result, the formula linking slopes k_{r1} and k_{r2} is required to eliminate these parameters. Hence,

$$\left(\frac{k_{f2} - k_{f1}}{\omega T} \right)^2 + (k_{r2})^2 = \left(\frac{V_{pk}}{L} \right)^2 + (\omega I_{pk})^2 \tag{4.40}$$

Subtracting Eq. (4.39) from Eq. (4.40) yields,

$$\frac{(k_{f2} - k_{f1})^2 - (k_{f1} - k_{f0})^2}{(\omega T)^2} = -\left(k_{r2}{}^2 - k_{r1}{}^2 \right) \tag{4.41}$$

Rearranging the above equation gives

$$(k_{f2} - k_{f1})^2 = (k_{f1} - k_{f0})^2 - (\omega T)^2 \cdot \left(k_{r2}{}^2 - k_{r1}{}^2 \right) \tag{4.42}$$

And,

$$k_{f2} = k_{f1} \pm \sqrt{(k_{f1} - k_{f0})^2 - (\omega T)^2 \cdot (k_{r2}^{\ 2} - k_{r1}^{\ 2})} \tag{4.43}$$

Due to the same reason stated before, Eq. (4.43) can be rewritten to eliminate the plus and minus sign in the equation,

$$k_{f2} = k_{f1} + sign(\cos \omega t) \cdot \sqrt{(k_{f1} - k_{f0})^2 - (\omega T)^2 \cdot (k_{r2}^{\ 2} - k_{r1}^{\ 2})} \tag{4.44}$$

In the above equation, variables k_{f0}, k_{f1}, and k_{r1} are the known slopes of the previous two successive switching periods k0 and k1. Variable k_{r2} can also be predicted and expressed by the known slopes k_{r0} and k_{r1}, see Eq. (4.32). In this sense, the slope of the second ramping segment k_{f2} can be predicted with the slopes in the previous two successive switching cycles without any knowledge of the circuit parameters.

4.2.4 Determination for the Desired Switching Instant

As discussed before, all the ramping slopes k_{r0}, k_{r1}, k_{f0}, and k_{f1} in the two successive switching cycles k1 and k0 can be detected from the measurements of the actual circuit parameters. Consequently, the two ramping slopes k_{r2} and k_{f2} in switching cycle k2 can be predicted and expressed in terms of these known slopes, see Eq. (4.32) and Eq. (4.44). After the two slopes k_{r2} and k_{f2} in switching cycle k2 have been obtained, a desired switching instant for switching period k2 can be derived.

The ramping slope k_{r2} and k_{f2} for switching cycle k2 are obtained according to Eq. (4.4) and (4.7) respectively, see Fig. 4.2.

$$k_{r2} = \frac{ierr_1(t_1) - ierr_2(t_0)}{t_1 - t_0} \tag{4.45}$$

$$k_{f2} = \frac{ierr_2(t_2) - ierr_1(t_1)}{t_2 - t_1} \tag{4.46}$$

Writing again the same control law that is used for model-based predictive current control scheme in the Chapter 3, gives,

$$ierr_1(t_1) = -ierr_2(t_2) \tag{4.47}$$

Substituting Eq. (4.47) into Eq. (4.46) gives

$$k_{f2} = \frac{-2 \cdot ierr_1(t_1)}{t_2 - t_1} \tag{4.48}$$

Rearranging the above equation gives,

$$ierr_1(t_1) = -\frac{k_{f2}(t_2 - t_1)}{2} \tag{4.49}$$

Also rearranging Eq. (4.45) gives,

$$t_1 - t_0 = \frac{ierr_1(t_1)}{k_{r2}} - \frac{ierr_2(t_0)}{k_{r2}} \tag{4.50}$$

Substituting Eq. (4.49) into Eq. (4.50) to eliminate the unknown $ierr_1(t_1)$ term,

$$t_1 - t_0 = -\frac{k_{f2}(t_2 - t_1)}{2k_{r2}} - \frac{ierr_2(t_0)}{k_{r2}} \tag{4.51}$$

Rearranging the above equation gives,

$$\left(1 - \frac{k_{f2}}{2k_{r2}}\right) t_1 = t_0 - \frac{k_{f2}}{2k_{r2}} t_2 - \frac{ierr_2(t_0)}{k_{r2}} \tag{4.52}$$

Hence,

$$t_1 = \left(t_0 - \frac{k_{f2}}{2k_{r2}} t_2 - \frac{ierr_2(t_0)}{k_{r2}}\right) \Big/ \left(1 - \frac{k_{f2}}{2k_{r2}}\right) \tag{4.53}$$

In the above equation, t_0 and t_2 are the fixed time instants once the switching frequency is determined. $ierr_2(t_0)$ designates the known magnitude of the current error signal at the start point of this switching cycle, for it is also the current error value of the end time instant in the previous switching cycle for the continuous current mode operation. The two slopes k_{r2} and k_{f2} predicted by the slopes of the previous two cycles are also known. In this sense, the desired switching instant t_1 can be predicted with Eq. (4.53). Consequently, the determination of the desired switching instant t_1 is based upon the current error slopes measured in real time, without involving any knowledge of the circuit parameters.

4.3 MATLAB Program Description

A MATLAB program is developed to verify the proposed current control scheme and is attached in Appendix B. Similar as the simulation program for model-based predictive control scheme, the single-phase rectifier bridge is adopted to examine the scheme in this program.

The maximum and minimum magnitudes of the current error signal are measured at time instants t_1 and t_2 respectively. Based upon these two values, slopes of the current error signal in one PWM switching cycle can be calculated. Consequently, in switching period k2, the slopes of the current error signal can be generated and the desired switching instant t_1 can be predicted.

The other two variables $ierr_2(t_0)$ and t_1, see Eq. (4.4) and Eq. (4.7), required for obtaining the values of the slopes, are assumed to be known. The variable $ierr_2(t_0)$ is the initial value of the current error in present switching cycle and is measured as $ierr_2(t_2)$ in the previous switching cycle. As for the time value t_1, it is predicted in the previous switching cycle and is known at the moment of calculation. Only the current values at two time instants t_1 and t_2 are required to be sampled in one PWM switching cycle. The time delay due to the ADC and DAC conversion time and the computational time is reduced, making this scheme suitable for DSP realization.

The switching time instant t_1 of the very first two switching cycles are given instead of being calculated. At the beginning of the operation, the bridge demands the switching on time as long as possible to increase the inductor current. In the MATLAB program, these two initial values of t_1 are given the values that are close to the full on time values of the switching cycle. In DSP implementation, these two cycles have to be tackled specially.

The performance of the current error signal at zero crossing is improved for this scheme. At the zero crossing in each line cycle, the current through the inductor reverses its direction. Due to this, the improper determination of the zero crossing based upon the supply voltage V_s produces the apparent deviations. An appropriate approach is to determine the zero crossing based on the sampled current error, other than that of the supply voltage. Whenever the magnitude of the current error reaches the lowest value around zero crossing, it is the right time to change the polarity of the modulated voltage pulse V_i. The change at this moment is expected

to bring the lowest impact to the change of the current direction through the inductor.

By nature, the inductor stores positive energy in the positive cycle. When the supply voltage V_s goes from positive to negative, the inductor current discharges the stored positive energy first and then reverses its direction. There is a slight time difference between the zero crossing of the supply voltage and that of the inductor current. The desired time for the modulated voltage pulse V_i to reverse its polarity is to change right after the inductor current fully discharged the stored positive energy so as to avoid the apparent deviations. This explanation is also applicable to the situation in the negative cycle.

4.4 Simulated Characteristics

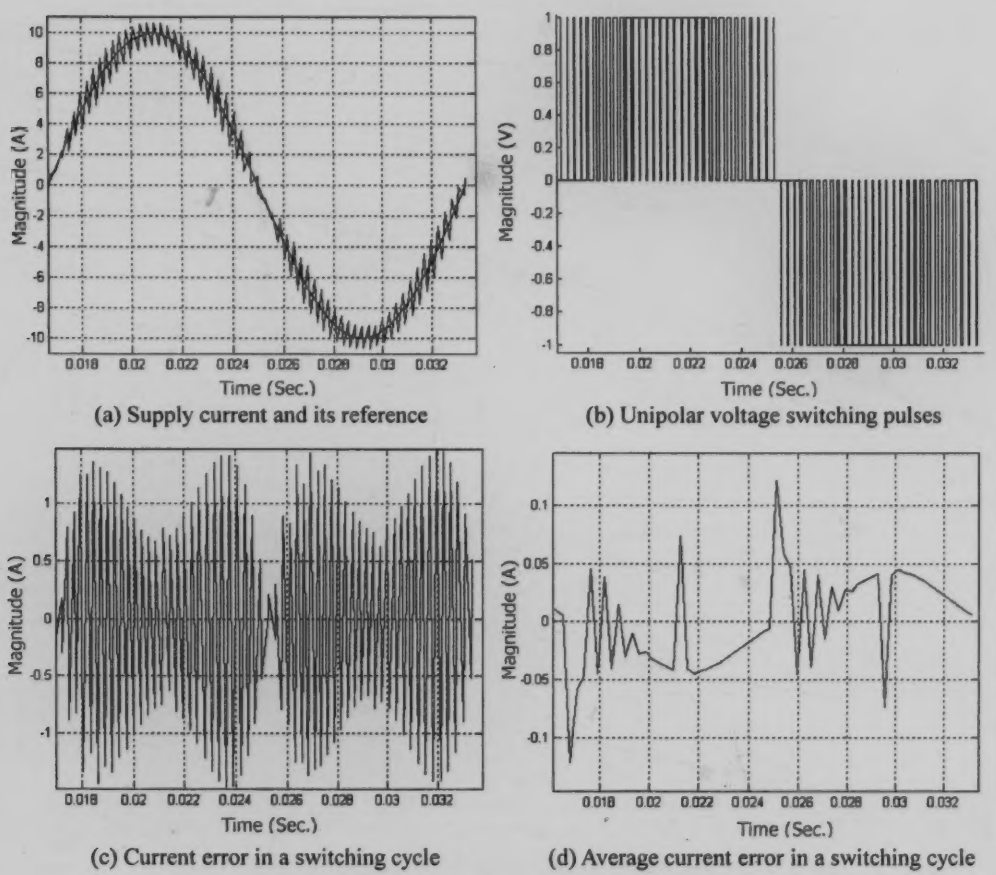
Slope detective current control scheme is examined using the single-phase PWM rectifier to verify the theoretical feasibility of the control algorithm. The simulations developed for examining the effectiveness of the proposed scheme are intended to have the control algorithm tested under the emulated practical experimental environment, which likely presents circuit parameters variations, noise interference and harmonics perturbations. Besides, transient response of this scheme based upon the change of the current reference is also investigated, for a stable and fast dynamic response is significant for practical applications of all control schemes. The switching frequency band is also analyzed to verify the performance in terms of constant switching frequency. The analysis of the supply current harmonic spectrum for almost all the examinations is introduced to make the analysis more straightforward.

4.4.1 Simulation Under the Nominal Condition

The simulation waveforms of the proposed scheme under the nominal condition are shown in Fig. 4.5. It is apparent that the supply current is centered on its current reference and the supply current ripple is centered on zero in a line cycle. The waveforms in Fig. 4.5 are simulated with the circuit parameters listed in Table 4.1, which is the same as those listed in table 3.1.

Table 4.1 Circuit parameters of the simulation waveforms in Fig. 4.5

Circuit Parameters	Values
Supply Inductance (L)	5mH
Supply Voltage (V_{pk})	169V, 60Hz
dc Link Voltage (E)	200V
Switching Frequency (f_{sw})	1800Hz
Clock Frequency	3600Hz
Current Reference (I_{ref})	10A



(a) Supply current and its reference

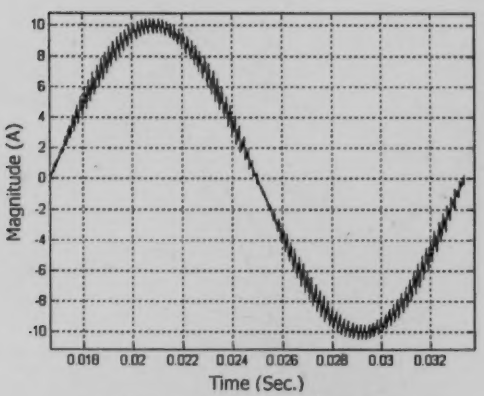
(b) Unipolar voltage switching pulses

(c) Current error in a switching cycle

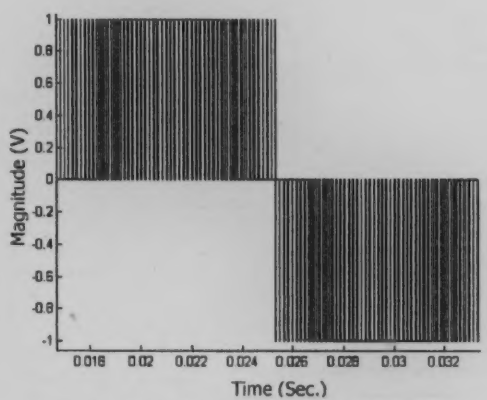
(d) Average current error in a switching cycle

Figure 4.5 Simulated waveforms under the nominal condition

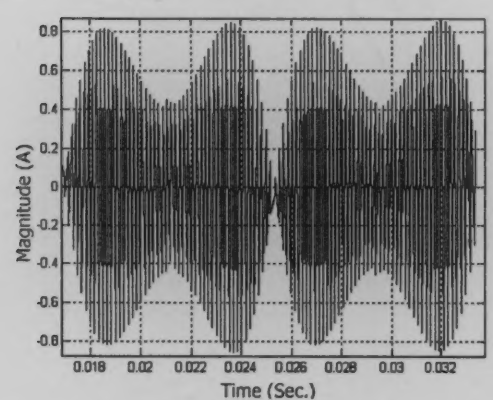
By observation, this control scheme has relative bigger average current error in comparison with model-based predictive control scheme under the same switching frequency, as shown in Fig. 4.5 (d) and Fig. 3.5 (d). This is attributed to the small signal linear simplification applied to the algorithm. A higher switching frequency truncates the modulated sinusoidal signal into more and smaller time intervals, satisfying the assumption of the small signal more accurate. The higher the switching frequency is, the better the performance it has. With a 3KHz switching frequency, the control scheme presents much smaller average current error excursions, as shown in Fig. 4.6 (d). Compared with the waveforms with an 1.8K switching frequency in Fig. 4.5, it is obvious that a higher switching frequency improves the performance of the proposed scheme.



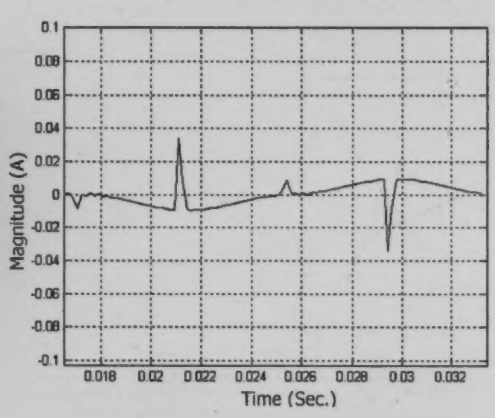
(a) Supply current and its reference



(b) Unipolar voltage switching pulses



(c) Current error in a switching cycle



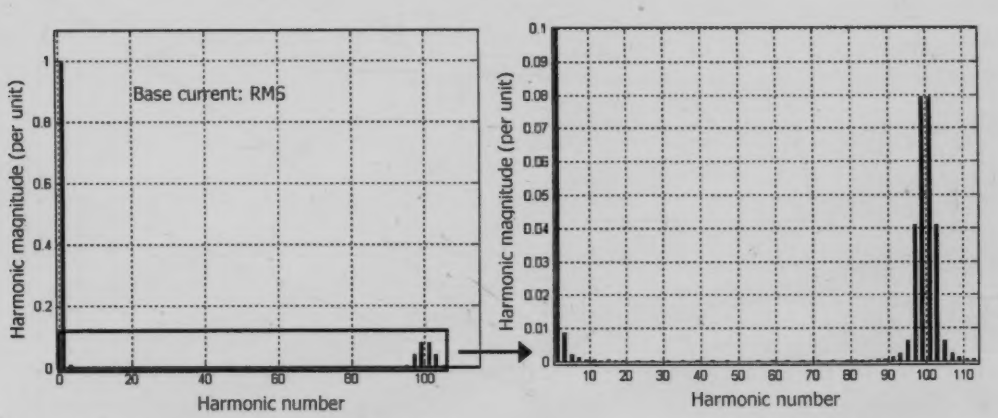
(d) Average current error in a switching cycle

Figure 4.6 Simulated waveforms with higher switching frequency

The determination of the zero crossing of model-based predictive control is based upon the supply voltage, other than the supply current. Hence model-based predictive control produces apparent deviations at zero crossing with a 3KHz switching frequency, as shown in Fig. 3.6, compared with the performance of slope detective control in Fig. 4.6. Slope detective control improves the performance of the zero crossing distortion, which is discussed in section 4.3.

Table 4.2 Circuit parameters of the simulated waveforms in Fig. 4.6

Circuit Parameters	Values
Supply Inductance (L)	5mH
Supply Voltage (V_{pk})	169V, 60Hz
dc Link Voltage (E)	200V
Switching Frequency (f_{sw})	*3000Hz*
Clock Frequency	*6000Hz*
Current Reference (I_{ref})	10A



(a) Harmonic spectrum of supply current (b) Expanded scale

Figure 4.7 Harmonic spectrum of the supply current in Fig. 4.6 (a) using fundamental of 60Hz

The supply current harmonic spectrum in Fig. 4.7 shows a low magnitude low order harmonics. This is ascribed to the existence of the apparent deviations of the average current

error, as shown in Fig. 4.6 (d). The two small deviations are due to the zero crossing distortion of the supply current. The two big deviations are due to the crest passing distortion of the supply voltage. It is attributed to the instantaneous slope polarity change of the supply voltage around crest. Higher switching frequency is desirable to attenuate unsatisfactory zero and crest crossing distortions with the price of the increased switching losses. Trade-off between the performance and the switching frequency is determined based upon the requirement of applications. The waveforms in Fig. 4.6 are simulated under the circuit condition listed in Table 4.2

4.4.2 Effect of the Circuit Parameter Variations

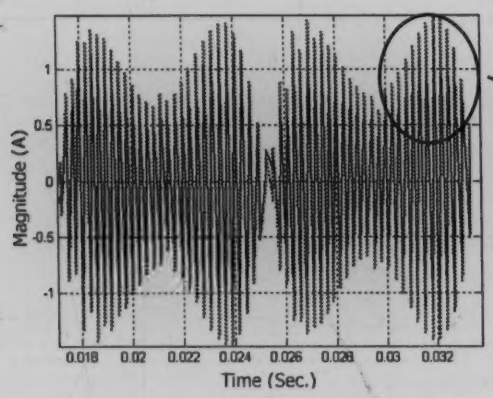
The effectiveness of the proposed control scheme about the circuit parameters variations is investigated. With 20% difference between the supply inductance, the supply current ripple waveform and the average current error waveform in two different cases exhibit very similar shapes but different amplitudes, as shown in Fig. 4.8. The very similar shapes of the two current error signals indicate that this scheme performs independent from circuit parameters variations, compared with the performance of mode-based control scheme in Fig. 3.6. No special designs for the control algorithm are necessary for applications with different circuit parameters.

Table 4.3 Different circuit parameters of the simulated waveforms in Fig. 4.8

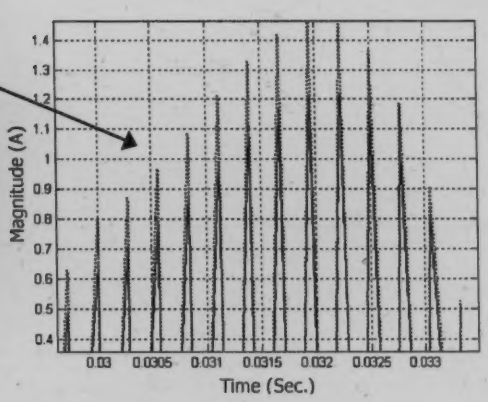
Circuit Parameters	Dotted Line	Solid Line
Supply Inductance (L)	*5mH*	*6mH*

The different amplitudes of the current error signals in Fig. 4.8 are due to the different values of the supply inductances used in the two simulation cases. Because the nature of the inductor is intended to limit current ripples in the circuit, a bigger inductance produces smaller amplitude of current ripples. In other words, if the control scheme could produce a smaller magnitude of the current error signal, it has the potential benefit of reducing the size of the supply inductance. The dotted line and the solid line in Fig. 4.8 designate different supply inductance cases respectively, as listed in Table 4.3. The rest of the simulation parameters are

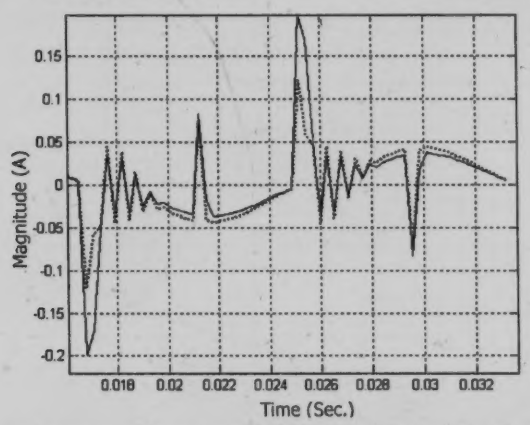
the same as those listed in Table 4.1.



(a) Supply currents with different inductance



(b) Expanded scale



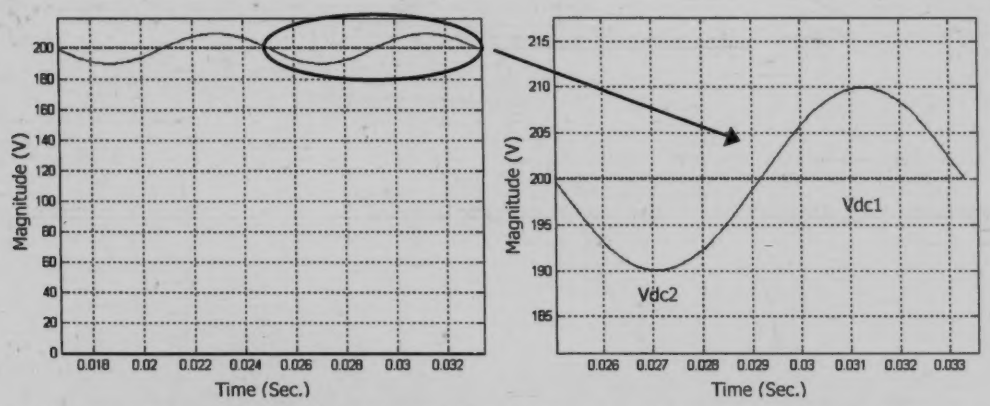
(c) Average current error waveforms, supply inductance: dotted line 5mH, solid line 6mH

Figure 4.8 Simulated waveforms with the different supply inductances

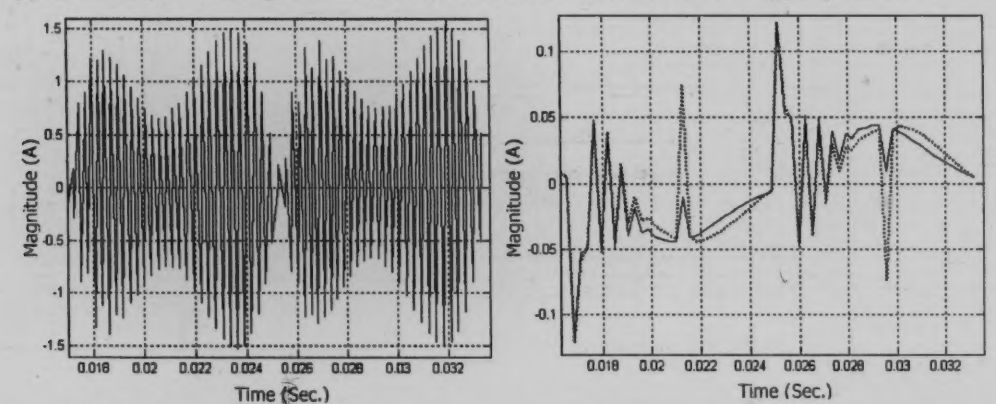
4.4.3 Effect of the dc Link Second Harmonic Voltage

The effectiveness of the proposed control scheme with the second harmonic injected in the dc link voltage is examined. Ideally, the controlled dc link voltage is kept constant at the desired dc voltage level. However, in practical, it is fairly hard to achieve that. The second harmonic is the predominant harmonic of the dc link voltage hence the effect of it is investigated here. The simulation waveforms in Fig. 4.9 show that the proposed scheme is strong enough to reject the variations of the dc link voltage. Unlike the performance of model-based predictive control

scheme in Fig. 3.7, the supply current ripple and the average current error waveforms in Fig. 4.9 exhibit almost the same shapes as those under the nominal case, disregarding the existence of the 5% second harmonic perturbations of the dc link voltage. The dotted line and the solid line in Fig. 4.9 indicate different dc link voltage cases, as listed in Table 4.4. The rest of the simulation parameters are the same as those listed in Table 4.1.



(a) Nominal 200V dc voltage and the one with 5% second harmonic variances (b) Expanded scale



(c) Current error in a switching cycle (d) Average current error in a switching cycle

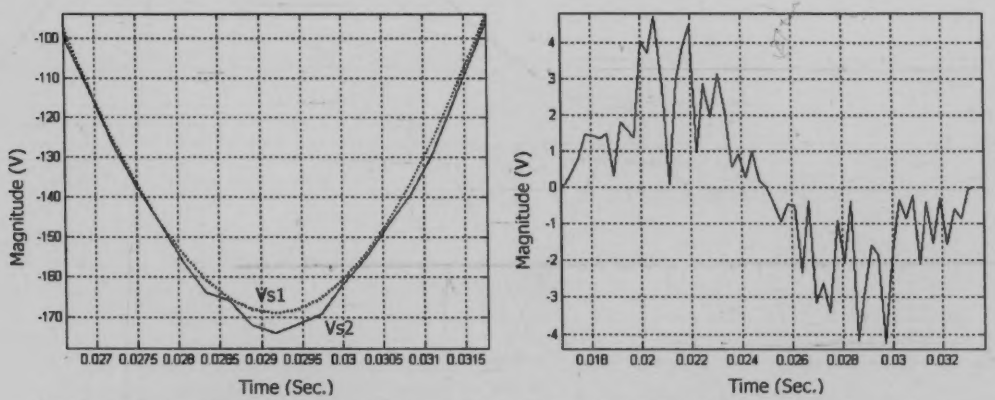
Figure 4.9 Waveforms with the injected 5% second harmonic in dc link voltage

Table 4.4 Different circuit parameters of the simulated waveforms in Fig. 4.9

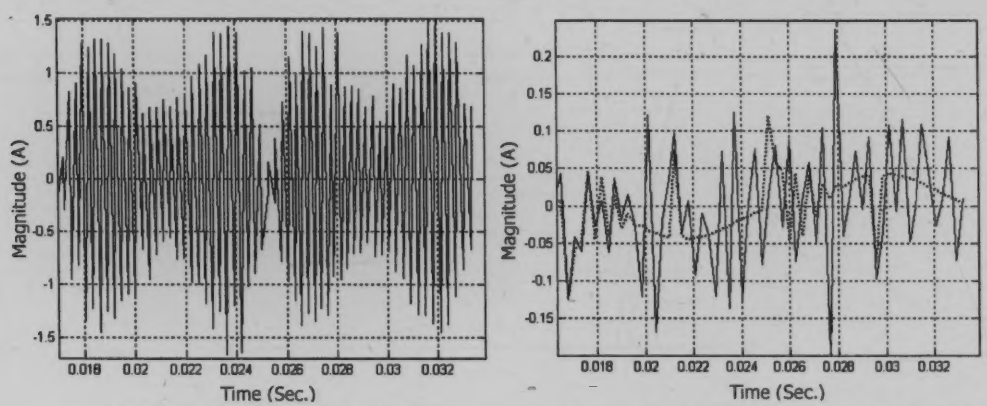
Circuit Parameters	Dotted Line	Solid Line
dc Link Voltage (E)	V_{dc1}: *200V*	V_{dc2}: *200-10*sin240πt V*

4.4.4 Effect of the Random Noise

The effectiveness of the proposed control scheme with the random noise in the ac supply voltage is investigated, for random noise is common and unavoidable during the practical experimental environment. It is apparent that the control algorithm is insensitive to the random noise interference, as shown in Fig. 4.10.



(a) Ideal supply voltage and the one with maximum 3% random noise (b) Injected random noise



(c) Current error in a switching cycle (d) Average current error in a switching cycle

Figure 4.10 Waveforms with 3% random noise in supply voltage

With maximum 3% random noise of the ac supply voltage, the average current error is still maintained around zero, despite the irregular shape indicating the existence of the random noise.

Comparing with the simulation waveform in Fig. 4.10 (d) and Fig. 3.8 (d), this scheme shows stronger noise rejection capability than mode-based predictive control scheme, for the average current error under the noise interference is still centered on zero for this scheme. The dotted line and the solid line in Fig. 4.10 indicate different ac supply voltage cases, as listed in Table 4.5. The rest of the simulation parameters are the same as those listed in Table 4.1.

Table 4.5 Different circuit parameters of the simulated waveforms in Fig. 4.10

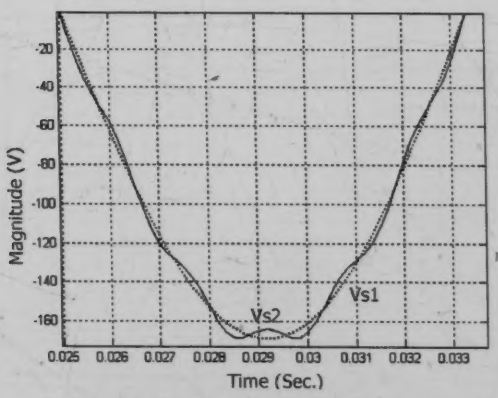
Circuit Parameters	Dotted Line	Solid Line
Supply Voltage (V_{pk})	V_{s1}: *169V, 60Hz*	V_{s2}: *169+5*rand V, 60Hz*

4.4.5 Effect of the ac Harmonic Voltages

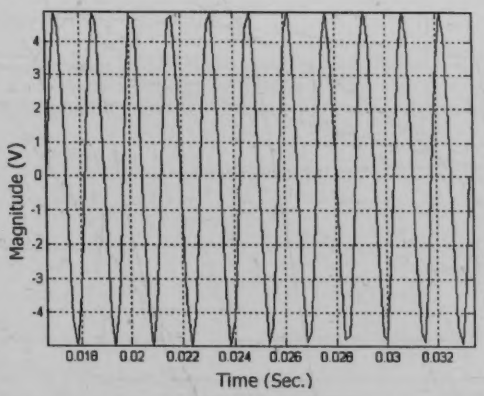
In practical, the expected sinusoidal ac supply voltage is often distorted by the ac harmonics produced by the other non-linear loads of the power system. The effectiveness of the proposed control scheme with the harmonic distorted ac supply voltage is examined. The eleventh harmonic, the third harmonic, and the second harmonic are injected into the ac supply voltage separately to test the control algorithm. It is shown that the control scheme has the controlled ac supply current followed its reference well enough in spite of the existence of the ac harmonic voltages, provided the magnitude of the harmonic voltage remains within the range of control, or the frequency of the harmonic voltage is not close to the switching frequency [35].

The first case examined here is the one with the 3% eleventh harmonic injected into the ideal ac supply voltage. Under this condition, the ac supply current is still centered on the current reference, see Fig. 4.11 (c) and (d). By observation, the supply current ripple and the average current error contain obvious the eleventh harmonic, as shown in Fig. 4.11 (e) and (f). This is also demonstrated by the significant increase of the eleventh harmonic in the supply current harmonic spectrum in Fig. 4.12, compared with that in the nominal condition in Fig. 4.7. It is clear that even with a small magnitude, the high order ac harmonic voltage could not be rejected completely if the harmonic frequency is quite close to the switching frequency, in this case around one fifth of the switching frequency. Higher switching frequency is demanded to

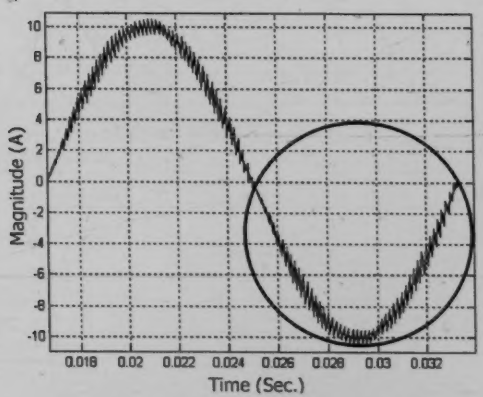
reduce the effect of the high frequency harmonic perturbations.



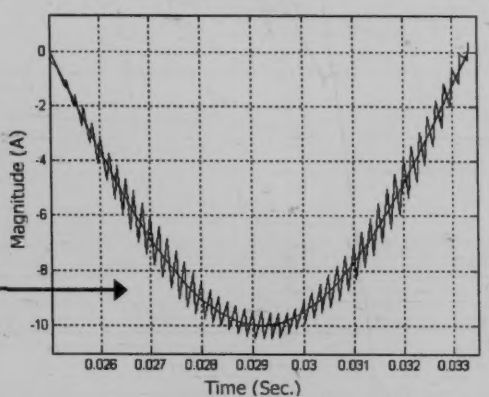
(a) Ideal supply voltage and the one with 3% 11th harmonic



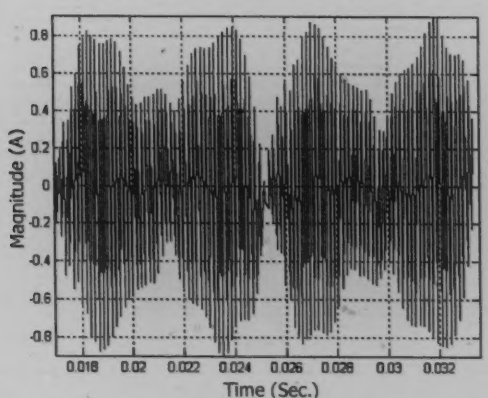
(b) the injected 3% eleventh harmonic



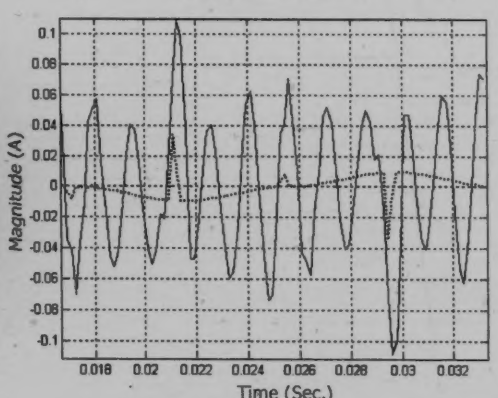
(c) Supply current and its reference



(d) Expanded scale



(e) Current error in a switching cycle

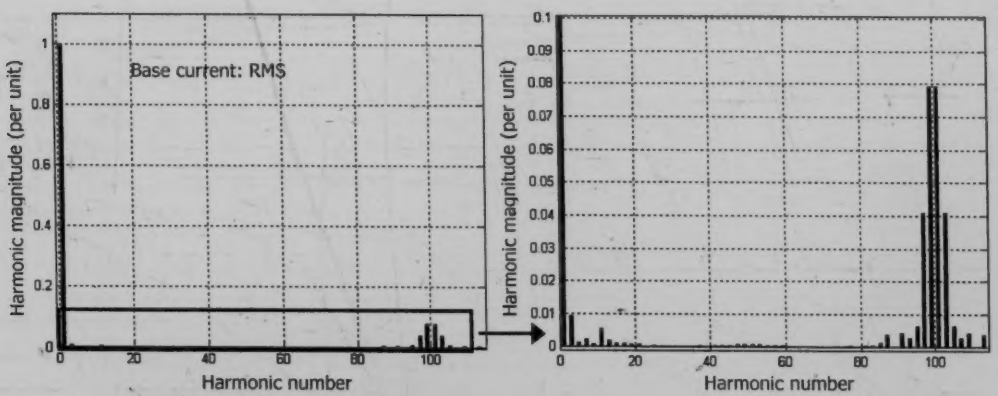


(f) Average current error in a switching cycle

Figure 4.11 Waveforms with 3% ac eleventh harmonic voltage

Table 4.6 Different circuit parameters of the simulated waveforms in Fig. 4.11

Circuit Parameters	Dotted Line	Solid Line
Supply Voltage Expression	V_{s1}: *169*sin120πt V*	V_{s2}: *169*sin120πt+5*sin1320πt V*



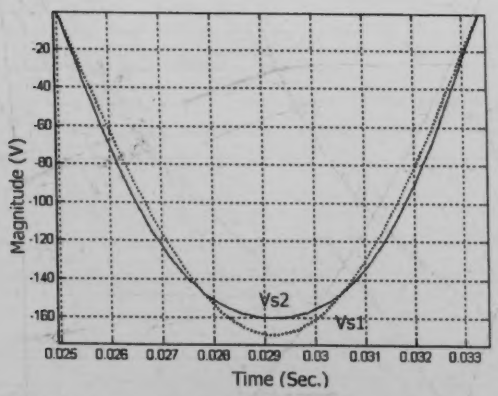
(a) Harmonic spectrum of supply current (b) Expanded scale

Figure 4.12 Harmonic spectrum of the supply current in Fig. 4.11 (c) using fundamental of 60Hz

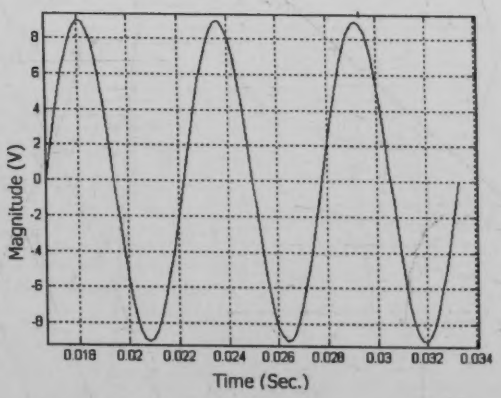
Further examination is carried by injecting around 5% third harmonic in the supply voltage to imitate the "flat top", a common distortion phenomenon of the supply voltage, as shown in Fig. 4.13 (a). The average current error in Fig. 4.13 (d) presents no significant excursions compared with the one under the nominal condition. The harmonic spectrum of the supply current in this case, as shown in Fig. 4.14, exhibits no obvious increase of the third harmonic, compared with that in the nominal condition in Fig. 4.7. Consequently, the proposed algorithm is strong at rejecting the ac harmonics with a relatively low frequency compared with the switching frequency. The dotted line and the solid line in Fig. 4.11 and Fig. 4.13 indicate different supply voltage cases, as listed in Table 4.6 and Table 4.7. The rest of the simulation parameters are the same as those listed in Table 4.3.

Table 4.7 Different circuit parameters of the simulated waveforms in Fig. 4.13

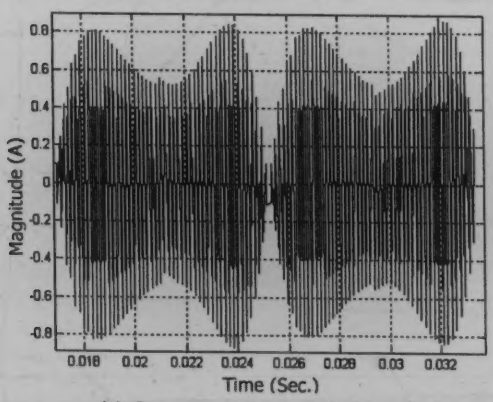
Circuit Parameters	Dotted Line	Solid Line
Supply Voltage Expression	V_{s1}: *169*sin120πt V*	V_{s2}: *169*sin120πt+9*sin360πt V*



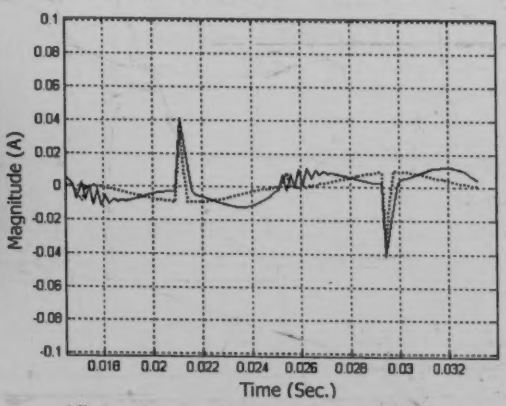
(a) Ideal supply voltage and the one with 5% 3rd harmonic



(b) Injected 5% 3rd harmonic

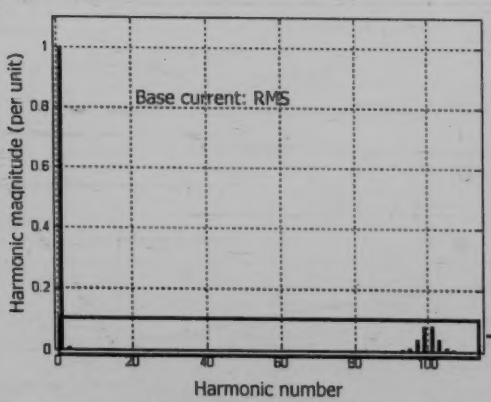


(c) Current error in a switching cycle

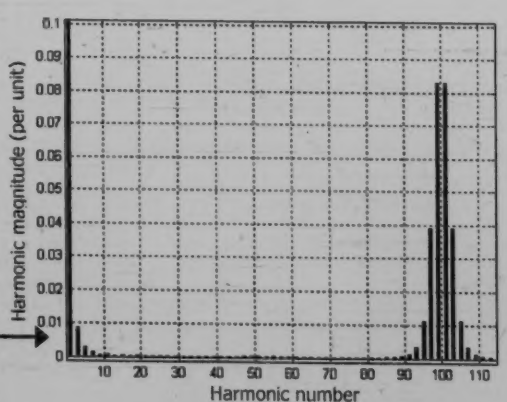


(d) Average current error in a switching cycle

Figure 4.13 Waveforms with 5% ac 3rd harmonic voltage

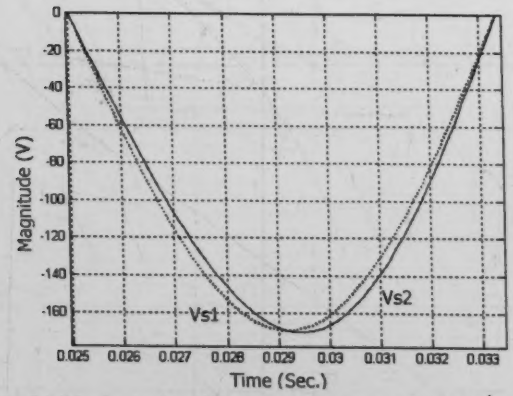


(a) Harmonic spectrum of the supply current

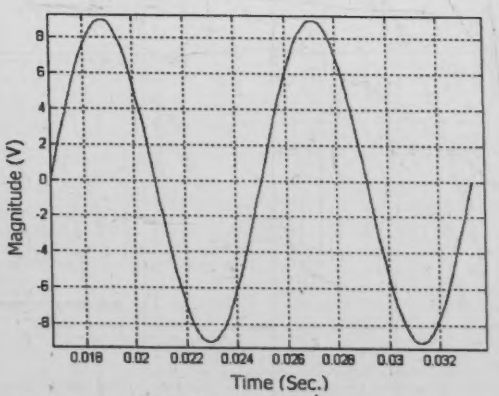


(b) Expanded scale

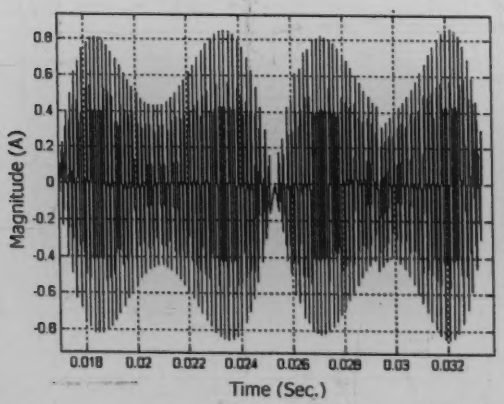
Figure 4.14 Harmonic spectrum of the supply current with 5% 3rd harmonic in the ac supply voltage



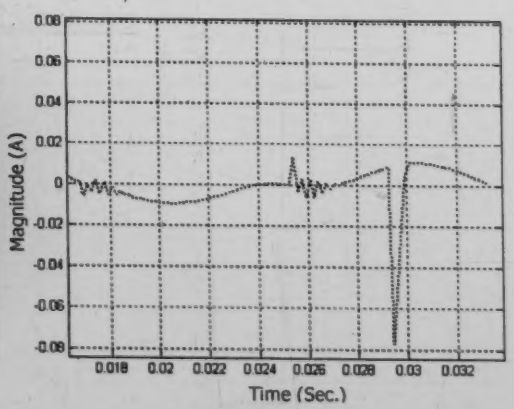
(a) Ideal supply voltage and the one with 5% 2nd harmonic



(b) Injected 5% 2nd harmonic

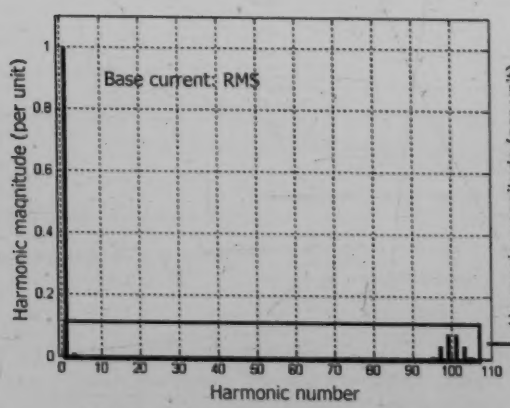


(c) Current error in a switching cycle

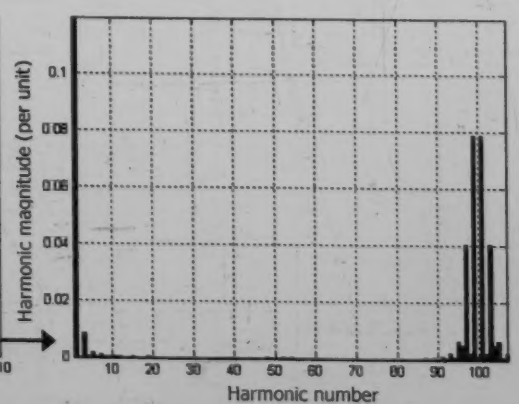


(d) Average current error in a switching cycle

Figure 4.15 Waveforms with 5% ac 2nd harmonic voltage



(a) Harmonic spectrum of the supply current



(b) Expanded scale

Figure 4.16 Harmonic spectrum of the supply current with 5% 2nd harmonic in the ac supply voltage

Table 4.8 Different circuit parameters of the simulated waveforms in Fig. 4.15

Circuit Parameters	Dotted Line	Solid Line
Supply Voltage Expression	V_{s1}: *169*sin120πt V*	V_{s2}: *169*sin120πt+10*sin240πt V*

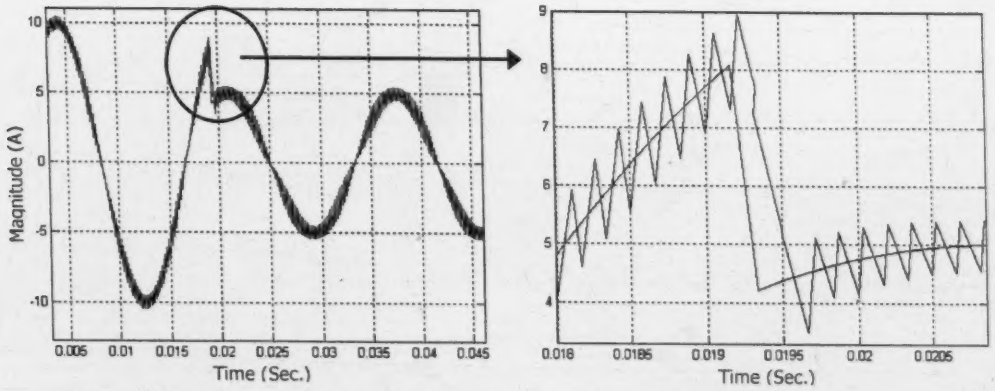
The supply voltage contains only odd harmonics if it is balanced and symmetrical with origin. Even harmonics make the supply voltage unbalanced and unsymmetrical in the positive and the negative half cycle. In this case, around 5% second harmonic is injected in ac supply voltage to test the proposed algorithm. The current error in Fig. 4.15 (c) presents no significant excursions and is centered on zero. The harmonic spectrum of the supply current in this case, as shown in Fig. 4.16, exhibits no second harmonic. Accordingly, the proposed control scheme has high immunity of the unbalanced supply voltage. The different supply voltage cases are listed in Table 4.8. The rest of the simulation parameters are the same as those listed in Table 4.3.

4.4.6 Transient Response

Transient response is significant performance to evaluate the practical feasibility of the proposed control scheme. Fast and stable dynamic performance is desired for all current control schemes. The transient response of the proposed control scheme is simulated by setting the half peak maganitude of the nominal current reference during its running process. The simulation parameters are listed in Table 4.9.

Table 4.9 Circuit parameters of the simulated waveforms in Fig. 4.17

Circuit Parameters	Values
Supply Inductance (L)	5mH
Supply Voltage (V_{pk})	169V, 60Hz
dc Link Voltage (E)	200V
Switching Frequency (f_{sw})	3000Hz
Clock Frequency	6000Hz
Current Reference (I_{ref})	*10A to 5A*



(a) Transient response of the supply current (b) Expanded scale

Figure 4.17 Transient response waveforms for the current reference change

By observation, the transient response of the proposed scheme is stable and fairly fast. It takes two switching cycles for the supply current to finish the transient response and regain the stable state operation, as shown in Fig. 4.17. At the instant of the transition, the dynaminc change could not be reflected immediately to the control algorithm since the prediction of the desired switching instant is based upon the current error slopes in the previous two successive switching cycles.

4.4.7 Switching Frequency Band

The digital-based slope detective current control scheme has an extremely narrow switching frequency band, as shown in Fig. 4.18. The start point and the end point in every switching period are always fixed time instants once the switching frequency is determined and is guaranteed by the digital clock rate. The well-regulated supply current is accomplished by the real-time adjusting and seeking for the desired switching instant between the fixed start and the end time instants. In practical, a slight excursion of the switching frequency band is possible due to the digital clock error and the other possible errors during implementation. The simulation parameters are listed in Table 4.3.

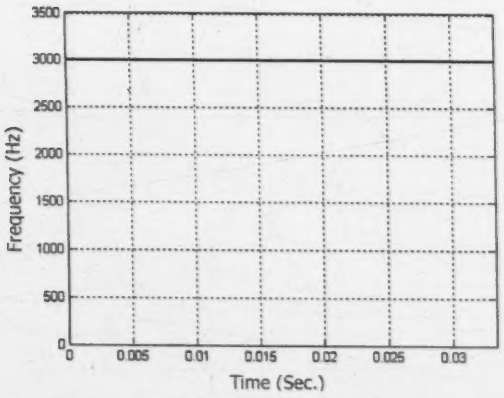


Figure 4.18 Extremely narrow switching band

4.5 Comparison with Other Current Control Schemes

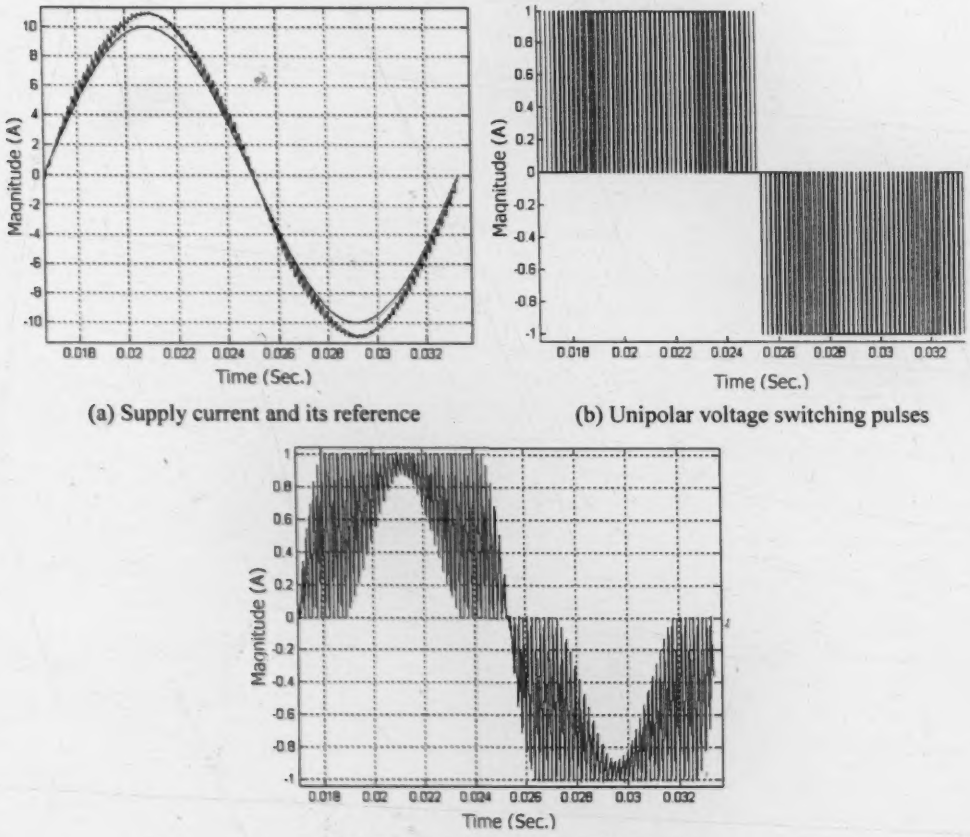
The foregoing discussions are concentrated on examinations of the performance of the proposed control algorithm under the different simulation conditions, emulating the practical circuit running environment. Investigations in this section are intended to prove the validation of the proposed control scheme by comparing its performance with those of other current control schemes that have been demonstrated experimentally. The comparison is intended to be given under the similar simulation environment for all the schemes. Two basic analogue control schemes, ramp comparison control [1-3], fixed band hysteresis control [20], and one digital control scheme, variable band hysteresis control [25], are examined and compared with the proposed control scheme.

4.5.1 Comparison with Ramp Comparison Control Scheme

Ramp comparison control scheme [1-3] is a very simple and stable analogue control scheme. This scheme features the constant switching frequency that avoids the occurrence of the undesirable white noise. It can be realized with very simple analogue components, such as comparators and subtracters, etc, without the real-time calculation of the switching instant that could only be fulfilled by the expensive and complex digital equipment. The MATLAB program

of this scheme is attached in Appendix C.

The simulation waveforms of ramp comparison control presented in Fig. 4.19 are simulated under the circuit condition listed in Table 4.10. Unipolar PWM scheme is adopted, as shown in Fig. 4.19 (b). In this case, the current error signal is directly compared with the triangular carrier reference, indicating that the proportional gain in this simulation condition is set at unity.



(a) Supply current and its reference

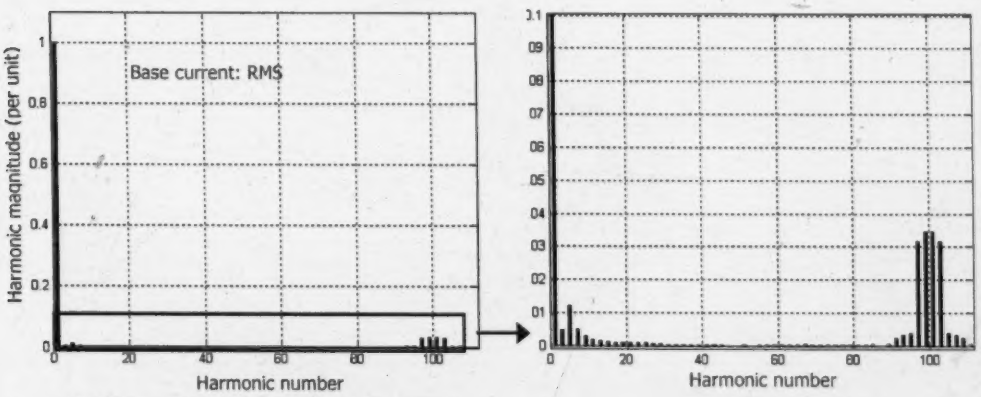
(b) Unipolar voltage switching pulses

(c) Current error in a switching cycle

Figure 4.19 Waveforms of ramp comparison control scheme

By observation, the supply current ripple is quite distorted within a line cycle compared with the symmetrical zero-centered current ripple of the proposed control scheme in Fig. 4.6 (c), indicating that the supply current does not follow the current reference precisely. This is also

verified by the harmonic spectrum of the supply current that presents the existence of the low order harmonics, as shown in Fig. 4.20. The predominant high order harmonics are around 6kHz, which is in coincidence with the general harmonic pattern of unipolar PWM control scheme.



(a) Harmonic spectrum of supply current (b) Expanded scale

Figure 4.20 Harmonic spectrum of the supply current in Fig. 4.19 (a) using fundamental of 60Hz

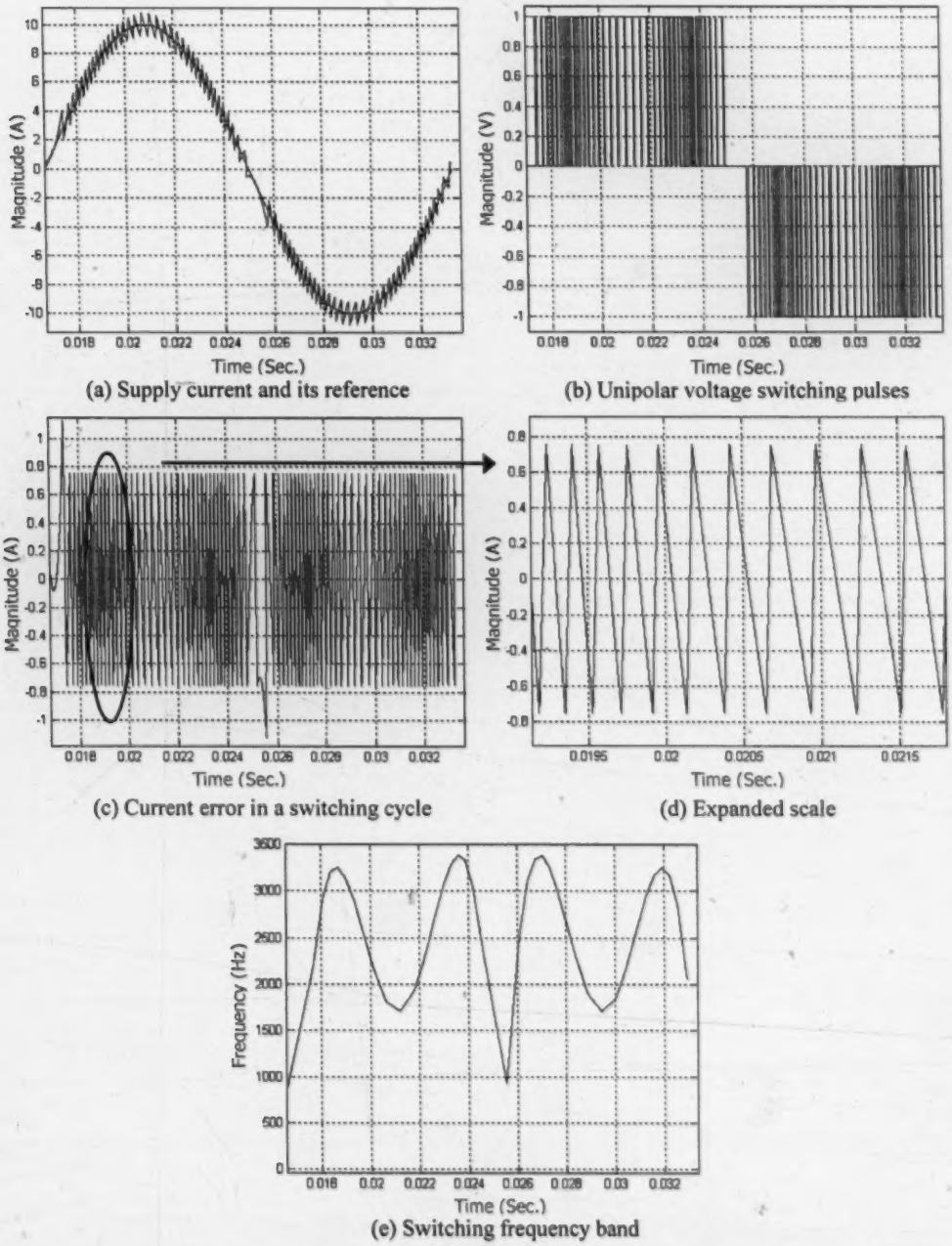
Table 4.10 Circuit parameters of the simulation waveforms in Fig. 4.19

Circuit Parameters	Values
Supply Inductance (L)	5mH
Supply Voltage (V_{pk})	169V, 60Hz
dc Link Voltage (E)	200V
Switching Frequency (f_{sw})	3000Hz
Current Reference (I_{ref})	10A

4.5.2 Comparison with Fix Band Hysteresis Control Scheme

Fix band hysteresis control scheme is also a simple analogue control scheme [20]. It attempts to regulate the current error within the pre-established fixed current band. Unipolar hysteresis control is adopted and accomplished by setting two current bands for the current

ripple signal. The inner current band controls the PWM pattern while the outer current band determines the pulse polarity. The MATLAB program of this scheme is attached in Appendix D.



(a) Supply current and its reference

(b) Unipolar voltage switching pulses

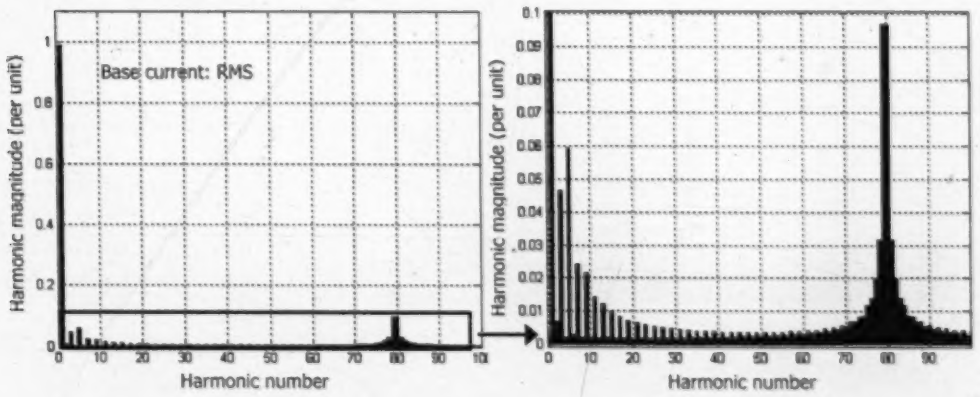
(c) Current error in a switching cycle

(d) Expanded scale

(e) Switching frequency band

Figure 4.21 Waveforms of fixed band hysteresis control scheme

Fix band unipolar hysteresis current control features with the well-regulated constant current error band, indicating that the supply current is controlled to follow the current reference without tracking errors. Just similar as the proposed control scheme in Fig. 4.6 (c), the current ripple of this control scheme is also centered on zero, as shown in Fig. 4.21 (c) and (d). However, comparing with the extremely narrow switching band of the proposed scheme in Fig. 4.18, this scheme shows a variable switching frequency in Fig. 4.21 (e). The variable switching frequency of this scheme is undesirable since it brings a large amount of low order harmonics.



(a) Harmonic spectrum of supply current (b) Expanded scale

Figure 4.22 Harmonic spectrum of the supply current in Fig. 4.21 (a) using fundamental of 60Hz

Table 4.11 Circuit parameters of the simulation waveforms in Fig. 4.21

Circuit Parameters	Values
Supply Inductance (L)	5mH
Supply Voltage (V_{pk})	169V, 60Hz
dc Link Voltage (E)	200V
Current Error Band	0.75A
Current Reference (I_{ref})	10A

The waveforms of fix band unipolar hysteresis current control in Fig. 4.21 are simulated

under the circuit condition listed in Table 4.11. The quite wide switching frequency band of this scheme in Fig. 4.21 (e) indicates the existence of the undesirable white noise. It is also revealed by the large amount of the low order harmonics in the harmonic spectrum of the supply current in Fig. 4.22, compared with that of the proposed scheme in Fig. 4.7. The white noise deteriorates the performance of the supply current in terms of low PF, high switching losses, extra harmonic heating problem, cost and design difficulty of the low order harmonic filter.

4.5.3 Comparison with Variable Band Hysteresis Control Scheme

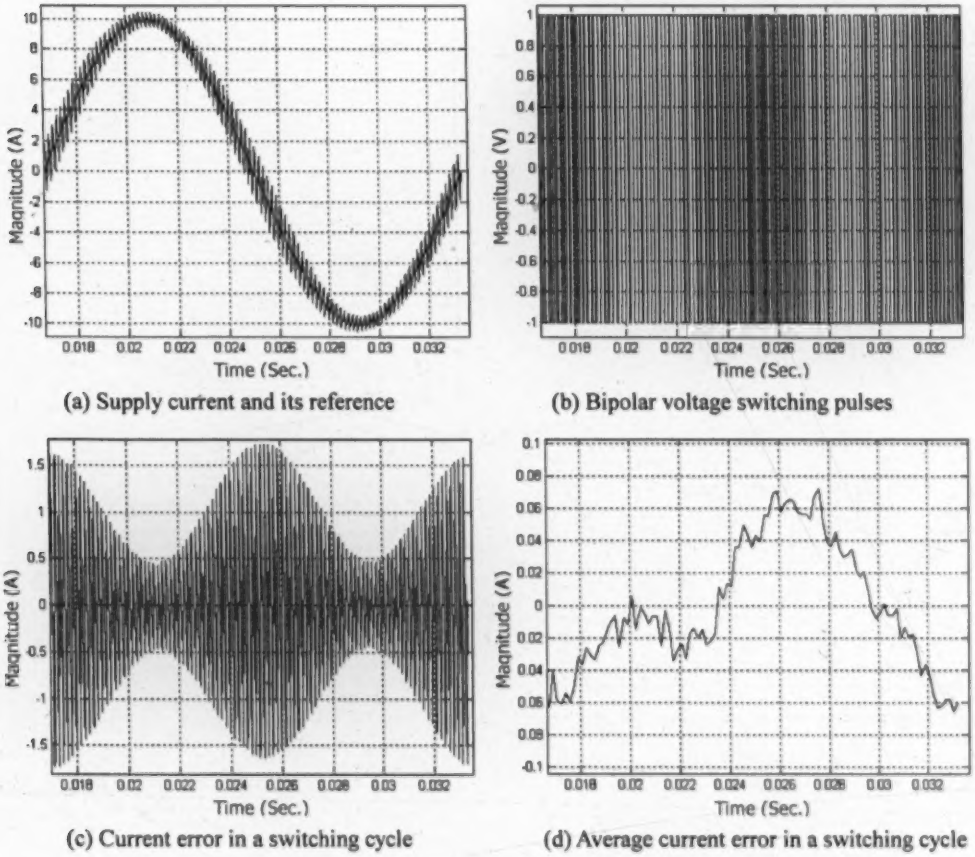
Variable band hysteresis control [25] is a digital-based current control scheme. It involves in the real-time calculation and prediction that could only be accomplished by the expensive and complex digital equipment. It is quite comparable in this manner with respect to the proposed control scheme. The detailed examinations about the performance of this scheme are given to compare with the proposed control scheme. The MATLAB program of this scheme is attached in Appendix E.

Table 4.12 Circuit parameters of the simulation waveforms in Fig. 4.23

Circuit Parameters	Values
Supply Inductance (L)	5mH
Supply Voltage (V_{pk})	169V, 60Hz
dc Link Voltage (E)	200V
Switching Frequency (f_{sw})	*6000Hz*
Clock Frequency	6000Hz
Current Reference (I_{ref})	10A

This control scheme attempts to generate the desired variable hysteresis band so as to maintain the constant switching frequency. The choice of the variable band is intended to eliminate the switching time error induced by the nonlinear hysteresis control algorithm. The prediction of the variable hysteresis band is based upon the positive and negative hysteresis

band and the time error in the previous successive switching period, referring to section 2.3.4.



(a) Supply current and its reference

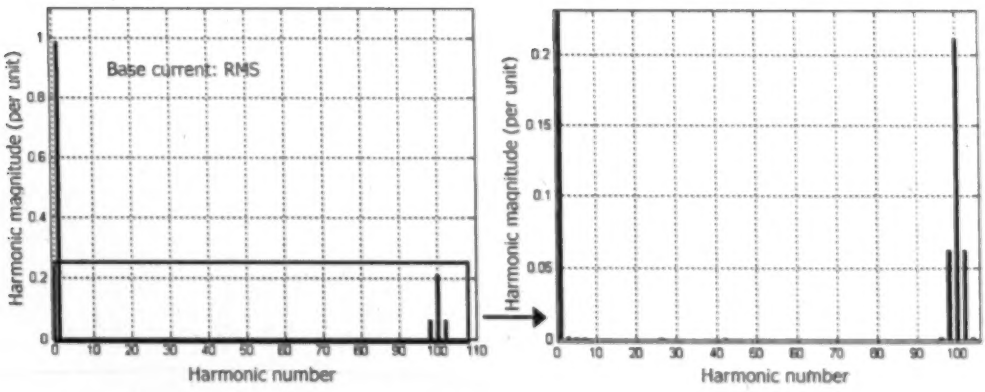
(b) Bipolar voltage switching pulses

(c) Current error in a switching cycle

(d) Average current error in a switching cycle

Figure 4.23 Waveforms of variable band hysteresis control scheme

The waveforms of variable band bipolar hysteresis current control in Fig. 4.23 are simulated under the circuit condition listed in Table 4.12. The simulated characteristics of this control scheme presents good performance in terms of the zero-centered current ripple and the fairly small amplitude of the average current error signal, as shown in Fig. 4.23 (c) and (d) respectively. However, the bipolar hysteresis control employed in this scheme brings forward a higher magnitude of the current ripple, compared with that of the proposed control algorithm with unipolar PWM scheme, as shown in Fig. 4.6 (c).

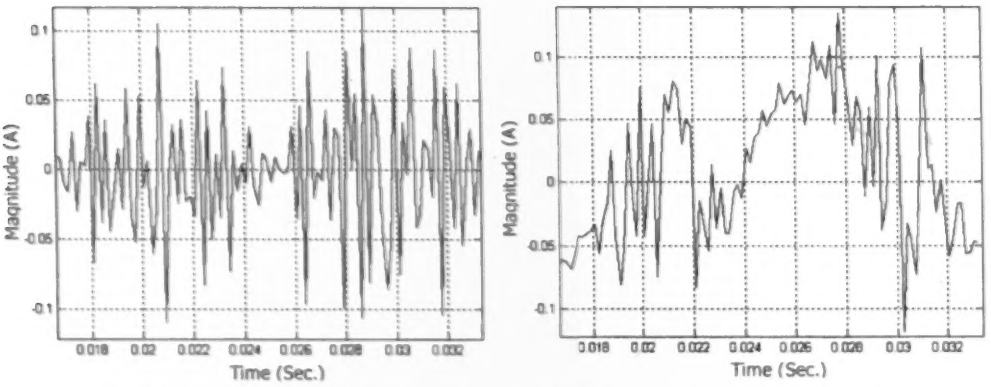


(a) Harmonic spectrum of supply current (b) Expanded scale

Figure 4.24 Harmonic spectrum of the supply current in Fig. 4.23 (a) using fundamental of 60Hz

With the 6KHz switching frequency, the maximum amplitude of the current ripple in a line cycle is beyond 1.5A, as shown in Fig. 4.23 (c). By simulation, a 12KHz switching frequency, four times as that of the proposed control scheme, is required to reduce the supply current ripple down to the same level as that of the proposed control scheme in Fig. 4.6 (c), within 10% (around 0.8A) of the reference current (10A). Comparing with this scheme, a smaller size of the supply inductor, or a lower switching frequency and hence lower switching losses are required as benefits of the proposed control scheme, provided the same level of the supply current ripple is demanded.

The supply current harmonic spectrum of this control scheme in Fig. 4.24 exhibits a larger amount of high order harmonics compared with those of the proposed scheme, as shown in Fig. 4.7. This is ascribed to bipolar PWM scheme adopted by this control algorithm. It also presents bigger supply current ripple compared with that of unipolar PWM slope detective control. As a result, the higher THD_f, about 16%, of this control scheme is produced, comparing with merely 9% THD_f of the proposed scheme. The predominant high order harmonics are around 6kHz, which is in coincidence with the general harmonic pattern of the bipolar hysteresis control scheme.

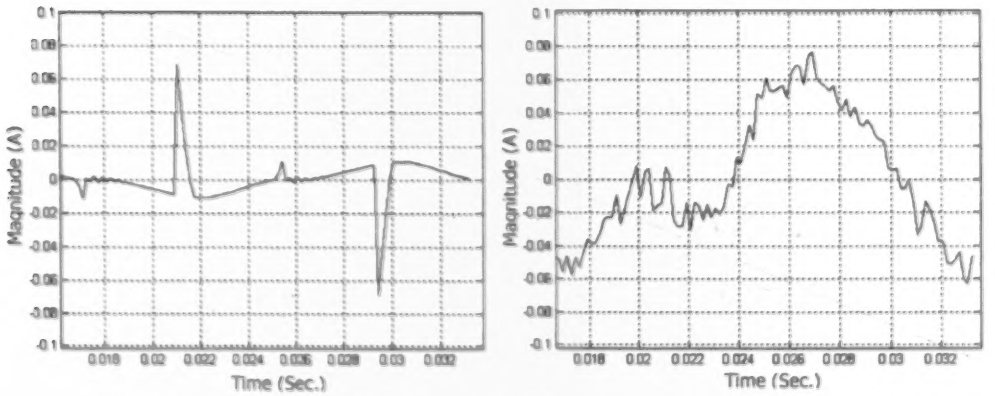


(a) Waveforms for slope detective control (b) Waveforms for variable hysteresis band control

Figure 4.25 Waveforms for both schemes with the maximum 3% random noise of the ac voltage

Table 4.13 Different circuit parameters of the simulated waveforms in Fig. 4.25

Circuit Parameters	For Fig. 4.25 (a)	For Fig. 4.25 (b)
Supply Voltage (V_{ph})	*169+5*rand V, 60Hz*	*169+5*rand V, 60Hz*
Switching Frequency (f_{sw})	*3000Hz*	*6000Hz*
Clock Frequency	*6000Hz*	*6000Hz*



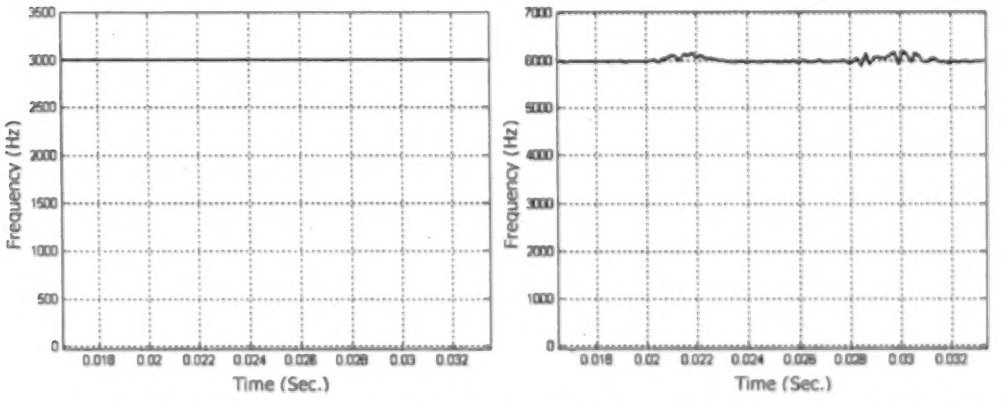
(a) Waveforms for slope detective control (b) Waveforms for variable hysteresis band control

Figure 4.26 Waveforms for both schemes with 5% 2nd harmonic of the dc link voltage

Table 4.14 Different circuit parameters of the simulated waveforms in Fig. 4.26

Circuit Parameters	For Fig. 4.26 (a)	For Fig. 4.26 (b)
dc Link Voltage (E)	*200-10*sin240πt V*	*200-10*sin240πt V*
Switching Frequency (f_{sw})	*3000Hz*	*6000Hz*
Clock Frequency	*6000Hz*	*6000Hz*

The effectiveness to resist the random noise in the ac supply voltage and the second harmonic in the dc link voltage is examined for both schemes. By observation of Fig. 4.25 and Fig. 4.26, the average current errors of both schemes in these two cases are of the similar shapes and amplitude ranges with those simulated under the nominal condition, as shown in Fig. 4.6 (d) and Fig. 4.23 (d) respectively. The strong capability to reject noise and harmonic perturbations is attributed to the real-time calculation and prediction techniques for both schemes.



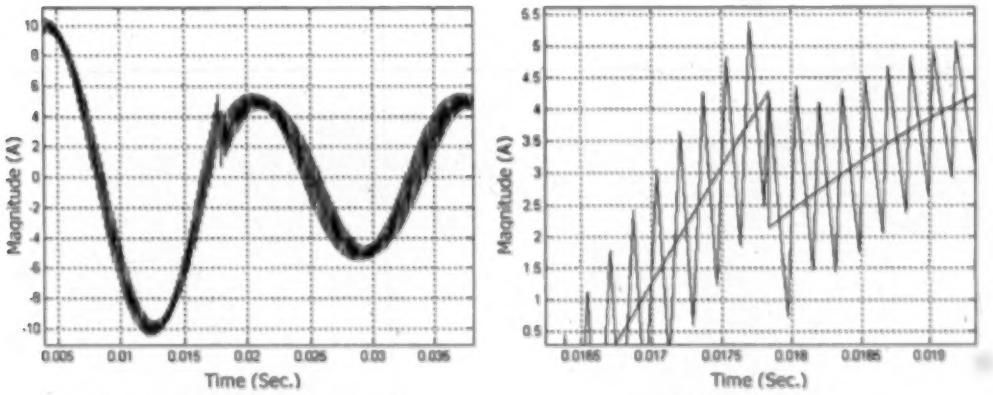
(a) Waveforms for slope detective control (b) Waveforms for variable hysteresis band control

Figure 4.27 Switching frequency band waveforms for both schemes

The variances in switching frequency of both schemes over the line cycle are depicted in Fig. 4.27. Variable band bipolar hysteresis control scheme has fairly narrow switching frequency band with respect to the extremely narrow switching frequency band of the proposed control scheme. The obvious excursions of the switching frequency of this control scheme occur around the crest points of the ac supply voltage. The occurrence of the time error is inevitable

and mainly attributed to the mechanism of the control scheme that always attempts to correct the time error after it appears.

As discussed in section 4.4.7, in practical, a slight excursion of the switching frequency band for the proposed control scheme is possible due to the digital clock error and the other possible errors during implementation. However, an even larger amount of excursion of the switching frequency band for this scheme, or say the similar hysteresis control schemes, is inevitable due to the same reason. The difference between these two are, for the proposed control scheme, the emphasis is on the fixed switching frequency. While for this scheme, the emphasis is on the variable hysteresis band. In this sense, the possible errors during the real realization that are mentioned above might probably be amplified and further introduce larger errors of the switching frequency in the practical implementation [25-27].



(a) Transient response of the supply current (b) Expanded scale

Figure 4.28 Transient response waveforms for the current reference change

The transient response of variable band hysteresis control scheme is quite fast, within one switching cycle as shown in Fig. 4.28 compared with that of the proposed control scheme in Fig. 4.17. This scheme determines the values of the both positive and negative hysteresis bands in one switching cycle separately, based upon the previous successive positive and negative hysteresis band values. It is possible for this scheme to adjust the hysteresis bands twice in one

switching cycle based on requirements. However, for the proposed control scheme, once the switching instant is determined, the control algorithm gives no update on the generated switching instant due to any dynamic change till the next cycle.

4.7 Summary

Slope detective current control scheme has been introduced. This scheme successfully achieves a symmetrical zero-centered current error by generating the desired switching instant based upon the slopes of the current error in the previous two successive PWM switching periods. The effectiveness of the control scheme is examined by using simulated characteristics and by comparing with three other control schemes.

From these efforts, it is apparent that the proposed scheme has an accurate control over the inductor current to force it to follow the current reference precisely. Other than the inductor current feedback, it eliminates the requirement of any knowledge of the circuit parameters to predict the desired switching instant. This scheme is independent of changes in circuit parameters. In addition, the transient response of this scheme is also stable and fairly fast.

This scheme is a digital-based fixed switching frequency unipolar PWM current control scheme. The fixed switching frequency is ensured by the DSP clock rate. Unipolar PWM scheme employed by this scheme produces low harmonics and low switching losses in the inductor current. Due to these features, the proposed control scheme is suitable for high power ac to dc or dc to ac applications. The requirement of sampling on the current error signal twice per PWM switching period makes this scheme very suitable for DSP implementation.

An imperfection of this scheme is the existence of some low magnitude low order harmonics. This is ascribed to the transients at the crest and zero crossing of the supply current. An improvement for these issues is expected to further refine the scheme. Besides, the proposed control scheme updates the control routine only once in every PWM switching cycle. Double updates of the control routine could introduce a faster transient response and are also expected to be further developed to improve the performance of the proposed control scheme.

Chapter 5 Conclusions

The steadily increasing utilization of power semiconductor utility rectifier has emphasized research attention on the resultant harmonic pollution of power systems. A PWM rectifier composed of switchable power transistors introduces full control of the ac supply current. Current control techniques applied to the PWM rectifier are investigated in this thesis to obtain accurate control and to minimize harmonic distortions in ac supply current. This thesis proposes two digital-based unipolar PWM control schemes that achieve a symmetrical zero-centered current error under the fixed switching frequency conditions for the single-phase PWM rectifier topology.

The current control techniques are briefly reviewed first and their relative merits are summarized in this chapter. Several possible future research topics are also discussed.

5.1 Review Main Work

Current control techniques applied to the PWM rectifier are generally catalogued into two classes: fixed switching frequency current control and hysteresis current control. The former scheme has a feature of constant switching frequency while regulating the current error signal to minimize the generation of harmonics. The latter scheme sets the band for the current error signal while managing the switching frequency to be fixed.

Current control techniques can be implemented in analogue or digital circuitry. An analogue implementation can be prone to noise interference and less accurate. For the control schemes based upon analogue realization, control accuracy is less satisfying. For instance, ramp comparison control produces a big distortion in inductor current signal around the crest points in a line cycle. Fixed band hysteresis current control introduces wide variations of the switching frequency. For the control schemes based upon digital implementation, the rectifier operation is improved but not as good as expected. For predictive current control, performance is not quite

satisfied when circuit parameters variations occur. For variable band hysteresis current control, variations of switching frequency cannot be completely eliminated.

New current control techniques are investigated due to limitations of many existing current control techniques. Model-based predictive current control has been proposed in this thesis. The main concept of this control scheme is to generate the desired switching instant based upon the pre-defined circuit model so as to achieve a symmetrical zero-centered current error in every PWM switching cycle. For this scheme, the switching frequency is always fixed and unipolar PWM is employed. A precise circuit model has to be developed before the control algorithm is applied. The switching instant is determined based upon the calculated inductor current in the previous switching period, the intended switching frequency, and the circuit parameters, such as V_{pk}, I_{pk}, E, L, which are given as long as the circuit model is developed. No current feedback loop is required for this control scheme.

The simulated characteristics for this scheme show that accurate current control is possible if no circuit parameters variations occur. Direct solutions for equations determining the switching instant are not given for this control scheme. However, it has the potential to be improved by involving the current feedback loop and implemented in analogue circuitry with multiplier and sine and cosine function generator. The main purpose of this control scheme in this thesis is to present a single-phase PWM rectifier bridge model, basic concepts and relevant formulas.

Slope detective current control scheme has been proposed in this thesis. The main idea for this control scheme is to predict the desired switching instant based upon the slopes of the current error signal in the previous two successive PWM switching cycles so as to achieve a symmetrical zero-centered current error signal. For this scheme, accurate control of the inductor current is accomplished. The switching frequency is guaranteed to be fixed by a digital clock. Unipolar PWM is employed to lower harmonic distortion and peak-to-peak current ripple with respect to bipolar PWM scheme. Only one current feedback loop is required, namely the inductor current.

Prediction on the desired switching instant can be made based upon the mathematical formulas. Two current error samples and corresponding numerical calculations per cycle are required. Essentially, the slope of the current error signal contains all the necessary information to take into account circuit parameters variations. The difference between the slopes of the current error signal in two successive switching cycles monitors the trend in circuit parameters changes. By sampling the slopes of the current error signal, and predicting the desired switching instant based upon it, the proposed control scheme achieves precise control in terms of symmetrical zero-centered current error, unity PF, extremely narrow switching frequency band, high immunity of the circuit parameters variations, strong capability to reject noises and harmonics perturbations, small amplitude of the current ripples, low harmonic distortions, low switching losses, stable and fairly fast transient response. Due to these features, the proposed control scheme is suitable for ac to dc or dc to ac power conversion applications, especially in high power rating and accurate control applications.

5.2 Future Work

While slope detective current control has lots of merits, more work is required to achieve the full benefit of the approach. The zero crossing distortion and the crest passing distortion of this scheme, discussed in Chapter 4, require further investigation to refine the algorithm. Though the performance of zero crossing distortion has been improved for this scheme, the crest passing distortion requires more attention.

On the other hand, the determination of the switching instant is based upon the predicted current slopes and only updates once in one PWM switching period. This limits the transient response speed of the proposed algorithm and as a result the deadbeat response is lost. A refinement is expected to give a second update in one switching period, especially in the case of the transient response.

In the cases of practical experimental implementation, some problems of the DSP realization are expected, e.g. digital time delay issues. This is probably caused by mainly two

reasons. One source of delay could be the delay due to the sampling time, ADC and DAC conversion time and relative propagation time. Another source could be the delay due to computational time. This latter issue could be solved properly by building a separate dedicate faster sampling and conversion hardware, further simplifying the scheme without degradation of the performance, or by employing advanced DSP hardware and software.

In practical, dead time is required for both switches on the same converter or inverter leg to commutate so as to avoid the occurrence of the circuit shortage. This dead time issue is not concerned in the simulation case and must be studied in the practical implementation.

Slope detective current control scheme presented in this thesis is verified by using a single-phase PWM rectifier bridge. An immediate extension of the control algorithm to the three-phase PWM rectifier bridge is feasible and applicable. Specific features of the three-phase system include a 120 degree phase delay of each phase, supply voltage unbalances. Careful study of these features may simplify the applications of the proposed algorithm in three-phase systems.

Bibliography

1. D. M. Brod, and D. W. Novotny, "Current control of VSI-PWM inverters", *IEEE Trans. Industrial Applications*, Vol. 21, No. 4, May/June 1985, pp. 562 – 570.
2. N. Mohan, T. M. Undeland, and W. P. Robbins, Power Electronics, Converters, Applications, and Design, Third Edition, John Wiley & Sons, INC.
3. J. Salmon, EE 530 Power Electronics Course Notes, Department of Electrical and Computer Engineering, Fall 2001.
4. M. Kazerani, P. D. Ziogas, and G. Joos, "A novel active current waveshaping technique for solid-state input power factor conditioners", *IEEE Trans. Industrial Electronics*, Vol. 38, No. 1, February 1991, pp. 72 – 78.
5. D. O'Sullivan, H. Spruyt, and A. Crausaz, "PWM conductance control", *IEEE PESC'88*, Vol. 1, April 1988, pp. 351 – 359.
6. L. Dixon, "Average current mode control of switching power supplies", in Unitrode Power Supply Design Seminar Handbook, 1990.
7. K. D. Purton, and R. P. Lisner, "Average current mode control in power electronic converters – analog versus digital", *AUPEC'02*, Melbourne, September 2002.
8. P. R. Holme, and C. D. Manning, "Digital control of high frequency PWM converters", *IEEE Proc., EPE'93*, Vol. 4, September 1993, pp. 260 – 265.
9. J. A. Gow, and C. D. Manning, "Novel fast-acting predictive current mode controller for power electronic converters", *IEE Proc. Electric Power Applications*, Vol. 148, No. 2, March 2001, pp. 133 – 139.
10. R. Wu, S. B. Dewan, and G. R. Slemon, "A PWM ac-to-dc converter with fixed switching frequency", *IEEE Trans. Industrial Applications*, Vol. 26, No. 5, September/October 1990, pp. 880 – 885.
11. O. Miyashita, U. Nishida, T. Ohnuki, E. Ohtsuji, and T. Haneyoshi, "High power factor PWM rectifiers with an analog pulse-width predictor", *IEEE APEC '94*, Vol.2, February

1994, pp. 563 – 568.

12. D. G. Holmes, and D. A. Martin, "Implementation of a direct digital predictive current controller for single and three phase voltage sources inverters", *IEEE IAS'96*, Vol. 2, October 1996, pp. 906 – 913.
13. T. Kawabata, T. Miyashita, and Y. Yamamoto, "Dead beat control of three phase PWM inverter", *IEEE Trans. Power Electronics*, Vol. 5, No. 1, January 1990, pp. 21 – 28.
14. L. Malesani, P. Mattavelli, and S. Buso, "Robust dead-beat current control for PWM rectifier and active filters", *IEEE Trans. Industrial Applications*, Vol. 35, No. 3, May/June 1999, pp.613 – 620.
15. Y. Sato, T. Ishizuka, K. Nezu, and T. Kataoka, "A new control strategy for voltage-type PWM rectifiers to realize zero steady-state control error in input current", *IEEE Trans. Industrial Applications*, Vol. 34, No. 3, May/June 1998, pp. 480 – 486.
16. H. Sugimoto, S. Moritomo, and M. Yano, "A high performance control method of a voltage-type PWM converter", *IEEE PESC'88*, Vol. 1, April 1988, pp. 360 – 368.
17. Y. Ye, M. Kazerani, and V. H. Quintana, "Modeling, control and implementation of three-phase PWM converters", *IEEE Trans. Power Electronics*, Vol. 18, No. 3, May 2003, pp. 857 – 864.
18. D. Lee, G. Lee, and K. Lee, "dc-bus voltage control of three-phase ac/dc PWM converters using feedback linearization", *IEEE Trans. Industrial Applications*, Vol. 36, No. 3, May/June 2000, pp. 826 – 833.
19. J. Dixon, S. Tepper, and L. Moran, "Practical evaluation of different modulation techniques for current-controlled voltage source inverters", *IEEE Proc. Electric Power Applications*, Vol. 143, No. 4, July 1996, pp. 301 – 306.
20. C. Gatlan, and L. Gatlan, "ac to dc PWM voltage source converter under hysteresis current control", *Industrial Electronics, ISIE '97*, Vol. 2, July 1997, pp. 469 – 473.
21. A. Tripathi and P. C. Sen, "Comparative analysis of fixed and sinusoidal band hysteresis current controllers for voltage source inverters", *IEEE Trans. Industrial Electronics*, Vol.

39, No. 1, February 1992, pp. 63 – 73.

22. M. N. Uddin, T. S. Radwan, G. H. George, and M. A. Rahman, "Performance of current controllers for VSI-fed IPMSM drive", *IEEE Trans. Industrial Applications*, Vol. 36, No. 6, November/December 2000, pp. 1531 – 1538.
23. Q. Yao and D. G. Holmes, "A simple, novel method for variable hysteresis band current control of a three phase inverter with constant switching frequency" *IEEE-IAS Annu. Meeting*, Oct. 1993, Vol.2, pp. 1122 – 1129.
24. T. W. Chun and M. K. Choi, "Development of adaptive hysteresis band current control strategy of PWM inverter with constant switching frequency," in *Proc. IEEE APEC'96*, San Jose, CA, 1996, pp. 194–199.
25. S. Buso, S. Fasolo, L. Malesani, and P. Mattavelli, "A dead-beat adaptive hysteresis current control", *IEEE Trans. Industrial Applications*, Vol. 36, No. 4, July/August 2000, pp. 1174 – 1180.
26. L. J. Borle, and C. V. Nayar, "Zero average current error controlled power flow for ac-dc power converters", *IEEE Trans. Power Electronics*, Vol. 10, No. 6, November 1995, pp. 725 – 732.
27. L. J. Borle, and C. V. Nayar, "Ramptime current control", *APEC '96*, Vol. 2, March 1996, pp: 828 – 834.
28. P. D. Ziogas, "The delta modulation techniques in static pwm inverters", *IEEE Trans. Industrial Applications*, Vol. 17, No. 2, March/April 1981, pp. 199 – 204.
29. M. A. Rahman, J. E. Quaicoe, and M. A. Choudhury, "Performance analysis of delta modulated PWM inverters", *IEEE Trans. Power Electronics*, Vol. 2, No. 3, July 1987, pp. 227 – 233.
30. C. F. Christiansen, M. I. Valla, and C. H. Rivetta, "A synchronization technique for static delta-modulated PWM inverters", *IEEE Trans. Industrial Electronics*, Vol. 35, No. 4, November 1988, pp. 502 – 507.
31. G. Joos, P. D. Ziogas, and D. Vincenti, "A model reference adaptive PWM technique",

IEEE Trans. Power Electronics, Vol. 5, No. 4, October 1990, pp. 485 – 494.

32. M. P. Kazmierkowski, and L. Malesani, "Current control techniques for three-phase voltage-source PWM converters: A survey", *IEEE Trans. Industrial Electronics*, Vol. 45, No. 5, October 1998, pp. 691 – 703.
33. S. Buso, L. Malesani, and P. Mattavelli, "Comparison of current control techniques for active filter applications", *IEEE Trans. Industrial Electronics*, Vol. 45, No. 5, October 1998, pp. 722 – 729.
34. H. L. Hess, "Power electronics instruction in the USA and Canada: topics, curricula and trends", *Int. J. Engng Ed.*, Tempus 1998, Vol. 14, No. 4, pp. 282 – 288.
35. L. J. Borle, "Zero average current error control methods for bi-directional ac-dc converters", Ph.D. dissertation, Curtin University of Technology, Bentley, Australia, October, 1999.

Appendix A

Program of Model-Based Predictive Current Control Scheme

```
clear;

freq=60;
N=60;
N1=3000;
period=1;
Vpk=169;
Ipk=10;
I0=0;
E0=200;
L=5e-3;
omega=2*freq*pi;
step=1/freq/N;
T0=0;
T2=step;
flag=1;
TT=(step-step/freq)*ones(1,period*N);
omegaL=omega*L;
a=Vpk/omegaL;
b=Ipk;

ieave=zeros(2,period*N);
ierr1=zeros(2,period*N);
ierr2=zeros(2,period*N);
IL1=zeros(2,period*N);
IL0=zeros(2,period*N);
Iref=zeros(2,period*N);

for i=1:(N*period)

    Iref(1,i)=T0;
    Iref(2,i)=Ipk*sin(omega*T0);
    Iref(2,period*N)=Ipk*sin(omega*step*period*N);
    Irefzc=sign(sin(omega*T0))*sign(sin(omega*T2));

    if Irefzc==-1
```

```
    flag=-flag;
  end;

  c=sign(flag)*E0/L;
  K=-a*cos(omega*T2)-c*T2+2*a*cos(omega*T0)-Ipk*sin(omega*T2)+2*I0;
  step1=step/N1;
    TD=0;

    for j=1:N1
        TD=TD+step1;
        T1=(i-1)*step+TD;
        xx=a*cos(omega*T1)-c*T1+b*sin(omega*T1);

        if abs(K-xx)<0.01
            TT(i)=TD;
        end;

     end;

   T1=(i-1)*step+TT(i);
   ierr1(1,i)=T1;  % calculate all values
   ierr1(2,i)=-a*(cos(omega*T1)-cos(omega*T0))-Ipk*sin(omega*T1)+I0;
   ierr2(1,i)=i*step;
   ierr2(2,i)=a*(cos(omega*T1)-cos(omega*T2))-Ipk*sin(omega*T2)-c*T2
              +c*T1 +ierr1(2,i)+Ipk*sin(omega*T1);
   ieave(1,i)=(T0+T2)/2;
   ieave(2,i)=(ierr1(2,i)+ierr2(2,i))/2;
   I1=ierr1(2,i)+Ipk*sin(omega*T1);
   I0=ierr2(2,i)+Ipk*sin(omega*T2);
   IL1(1,i)=T1;
   IL1(2,i)=I1;
   IL0(1,i)=i*step;
   IL0(2,i)=I0;
   I2=I0;
   T0=T2;
   T2=T2+step;
end;

figure (1); clf;
ierr=zeros(2,2*period*N);
```

```
for i=1:2*period*N

   if mod(i,2)==1
      ierr(1,i)=ierr1(1,(i+1)/2);
      ierr(2,i)=ierr1(2,(i+1)/2);
   else
      ierr(1,i)=ierr2(1,i/2);
      ierr(2,i)=ierr2(2,i/2);
   end;

end;

plot(ierr(1,:),ierr(2,:));
grid on;

figure (2); clf;
plot(ieave(1,:),ieave(2,:));
grid on;

figure (3); clf;
IL=zeros(2,2*period*N);

for i=1:2*period*N

   if mod(i,2)==1
      IL(1,i)=IL1(1,(i+1)/2);
      IL(2,i)=IL1(2,(i+1)/2);
   else
      IL(1,i)=IL0(1,i/2);
      IL(2,i)=IL0(2,i/2);
   end;

end;

plot(IL(1,:),IL(2,:));
hold on;
plot(Iref(1,:),Iref(2,:),'r');
hold off;
grid on;
```

Appendix B

Program of Slope Detective Current Control Scheme

```
clear;

freq=60;
N=150;
period=1;
Vpk=169;
Ipk=10;
I0=0;
E0=200;
L=5e-3;
omega=2*freq*pi;
step=1/freq/N;
T0=0;
T2=step;
T=step/freq;
T1=T2-T;
flag=1;
flag3=0;
omegaL=omega*L;
a=Vpk/omegaL;
b=Ipk;
h=omega*step;

Kr=zeros(1,period*N);
Kf=zeros(1,period*N);
ierr1=zeros(2,period*N);
ierr2=zeros(2,period*N);
IL1=zeros(2,period*N);
IL0=zeros(2,period*N);
Iref=zeros(2,period*N+1);

Iref(1,N*period+1)=step*N*period;
Iref(2,N*period+1)=Ipk*sin(omega*step*N*period);

for i=1:(N*period)
   Iref(1,i)=T0;
```

```
Iref(2,i)=Ipk*sin(omega*(T0));
flag2=sign(sin(omega*T2)-sin(omega*T0));
c=sign(flag)*E0/L;
ierr1(1,i)=T1;  % calculate all values
ierr1(2,i)=-a*(cos(omega*T1)-cos(omega*T0))-Ipk*sin(omega*T1)+I0;
ierr2(1,i)=i*step;
ierr2(2,i)=a*(cos(omega*T1)-cos(omega*T2))-Ipk*sin(omega*T2)-c*T2
          +c*T1+ierr1(2,i)+Ipk*sin(omega*T1);
ieave(1,i)=(T0+T2)/2;
ieave(2,i)=(ierr1(2,i)+ierr2(2,i))/2;
I1=ierr1(2,i)+Ipk*sin(omega*T1);
I0=ierr2(2,i)+Ipk*sin(omega*T2);
IL1(1,i)=T1;
IL1(2,i)=I1;
IL0(1,i)=i*step;
IL0(2,i)=I0;

if i==1
   Kr(i)=(ierr1(2,i)-0)/(T1-T0);
   Kf(i)=(ierr2(2,i)-ierr1(2,i))/(T2-T1);
else
   Kr(i)=(ierr1(2,i)-ierr2(2,i-1))/(T1-T0);
   Kf(i)=(ierr2(2,i)-ierr1(2,i))/(T2-T1);
end;

if i>1
   Kr(i+1)=Kr(i)*(1-h*h/2)-h*h*(1-h*h/8)*(Kr(i)^2-Kr(i-1)^2)))
           +flag2*sqrt(abs((Kr(i)-Kr(i-1)*(1-h*h/2))^2;
   Kf(i+1)=flag2*sqrt(abs((Kf(i)-Kf(i-1))^2-h*h*(Kr(i)-Kr(i-1))^2
           +Kf(i)+((Kr(i))^2-(Kr(i-1))^2)*h^4));
end;

if i==1
   T1next=T2+step-T;
end;

if (i<(N*period))&&(i>1)
   T1next=(T2-Kf(i+1)*(T2+step)/2/Kr(i+1)-ierr2(2,i)/Kr(i+1))
          /(1-Kf(i+1)/2/Kr(i+1));

   if (T1next>T2+step)
```

```
            T1next=T2+step-T;
        end;

    end;

    ierr1(2,i+1)=-a*(cos(omega*T1next)-cos(omega*T2))
                 -Ipk*sin(omega*T1next)+I0;
    ierr2(2,i+1)=a*(cos(omega*T1next)-cos(omega*(T2+step)))+c*T1next
                 -c*(T2+step)-Ipk*sin(omega*(T2+step))+ierr1(2,i)
                 +Ipk*sin(omega*T1next);

    if ((ierr1(2,i+1)/ierr1(2,i))<0)&&(i>N/3)
        flag=-flag;
        flag3=2;
    end;

    if (flag3==2)||(flag3==1)
        T1next=(-ierr2(2,i)/Kr(i+1)+T2+Kf(i+1)*(T2+step)/2/Kr(i+1))
               /(1+Kf(i+1)/2/Kr(i+1));

        if (T1next>T2+step)
            T1next=T2+step-T;
        end;

        flag3=flag3-1;

    end;

    I2=I0;
    T0=T2;
    T1=T1next;
    T2=T2+step;

end;

figure (1);
ierr=zeros(2,2*period*N);

for i=1:2*period*N

    if mod(i,2)==1
```

```
        ierr(1,i)=ierr1(1,(i+1)/2);
        ierr(2,i)=ierr1(2,(i+1)/2);
    else
        ierr(1,i)=ierr2(1,i/2);
        ierr(2,i)=ierr2(2,i/2);
    end;

end;

plot(ierr(1,:),ierr(2,:),'b');
grid on;
hold on;

figure(2);
plot(ieave(1,:),ieave(2,:),'b');
hold on;
grid on;

figure (3);
IL=zeros(2,2*period*N);
IL(1,1)=0;
IL(2,1)=0;

for i=1:2*period*N
    j=i+1;

    if mod(j,2)==0
        IL(1,j)=IL1(1,(i+1)/2);
        IL(2,j)=IL1(2,(i+1)/2);
    else
        IL(1,j)=IL0(1,i/2);
        IL(2,j)=IL0(2,i/2);
    end;

end;

plot(IL(1,:),IL(2,:));
hold on;
plot(Iref(1,:),Iref(2,:),'r');
hold off;
grid on;
```

Appendix C

Program of Ramp Comparison Current Control Scheme

```
clear;

fsw=3000;
omegasw=2*pi*fsw;
freq=60;
omega=2*pi*freq;
oriang=270/180*pi;
coef=1/1.5683;
periodsw=fsw/freq;
periodsin=1;
step=1/fsw;
N=1000;
step1=step/N;
T=step1;
L=5e-3;
Vpk=169;
Ipk=10;
E=200;
omegaL=omega*L;
a=Vpk/omegaL;
c=E/L;
flag=-1;

trig=zeros(2,N*periodsin*periodsw);
Iref=zeros(1,N*periodsin*periodsw);
pulse=zeros(1,N*periodsin*periodsw);
pulsea=zeros(1,N*periodsin*periodsw);
pulseb=zeros(1,N*periodsin*periodsw);
I=zeros(1,N*periodsin*periodsw);
ierr=zeros(1,N*periodsin*periodsw);
pulse(1,1)=0;

for i=1:(N*periodsin*periodsw)
    trig(1,i)=T;
    trig(2,i)=coef*asin(sin(omegasw*T+oriang));
    Iref(1,i)=Ipk*sin(omega*T);
```

```
    if i==1
       I(1,1)=-a*cos(omega*T)+a-c*T*pulse(1,1);
    else
       I(1,i)=I(1,i-1)-a*(cos(omega*T)-cos(omega*(T-step1)))
              -c*step1*pulse(1,i);
    end;

    ierr(1,i)=I(1,i)-Iref(1,i);

    if (ierr(1,i)>trig(2,i))&&(i<N*periodsin*periodsw)
        pulsea(1,i+1)=1;
    else pulsea(1,i+1)=0;
    end;

    if (-ierr(1,i)>trig(2,i))&&(i<N*periodsin*periodsw)
        pulseb(1,i+1)=1;
    else pulseb(1,i+1)=0;
    end;

    if i<N*periodsin*periodsw
       pulse(1,i+1)=pulsea(1,i+1)-pulseb(1,i+1);
    end;

    T=T+step1;

end;

figure (1);clf;
plot (trig(1,:),I(:));
hold on;
plot (trig(1,:), Iref(:),'r');
grid on;

figure (2);clf;
plot (trig(1,:),ierr(:));
grid on;
```

Appendix D

Program of Fixed Band Hysteresis Current Control Scheme

```
clear;

freq=60;
N=100000;
period=1;
Vpk=169;
Ipk=10;
E0=200;
L=5e-3;
omega=2*freq*pi;
step=1/freq;
step1=step/N;
ierrband=0.8;
bandcoef=1.5;
ierrbandex=bandcoef*ierrband;
T=step1;
k=2;
j=1;
flag=1;
omegaL=omega*L;
pflag=0;
nflag=0;
a=Vpk/omegaL;
b=Ipk;
c=E0/L;

ierr=zeros(1,period*N);
ierrL=zeros(1,period*N);
Iref=zeros(1,period*N);
I=zeros(1,period*N);
pulse=zeros(1,period*N);
pulsea=zeros(1,period*N);
pulseb=zeros(1,period*N);
time=zeros(1,period*N);
tm=zeros(1,period*N);
IL=zeros(1,period*N);
```

```
pulse(1,1)=0;
pulsea(1,1)=0;
pulseb(1,1)=0;

for i=1:(N*period)
    time(1,i)=T;
    Iref(1,i)=Ipk*sin(omega*T);

    if i==1
       I(1,1)=-a*cos(omega*T)+a-c*T*pulse(1,1);
    else
       I(1,i)=I(1,i-1)-a*(cos(omega*T)-cos(omega*(T-step1)))
              -c*step1*pulse(1,i);
    end;

    ierr(1,i)=I(1,i)-Iref(1,i);

    if     ierr(1,i)>ierrbandex
           pulseb(1,i+1)=0;
    elseif  ierr(1,i)<-ierrbandex
           pulseb(1,i+1)=1;
    else
           pulseb(1,1+i)=pulseb(1,i);
    end;

    if     (ierr(1,i)>ierrband)&&(pflag==0)
              pulsea(1,i+1)=1;
    elseif  (ierr(1,i)<-ierrband)&&(nflag==0)
              pulsea(1,i+1)=0;
    else
           pulsea(1,1+i)=pulsea(1,i);
    end;

    if i<N*period
       pulse(1,i+1)=pulsea(1,i+1)-pulseb(1,i+1);
    end;

    T=T+step1;

end;
```

```
figure (1);clf;
plot (time(:),ierr(:));
grid on;

figure (2); clf;
plot (time(:), Iref(:),'r');
hold on;
grid on;
plot (time(1,:), I(:));
```

Appendix E

Program of Variable Band Hysteresis Current Control Scheme

```
clear;

freq=60;
N=100000;
period=1;
Vpk=169;
Ipk=10;
E0=200;
L=5e-3;
omega=2*freq*pi;
step=1/freq;
step1=step/N;
T=step1;
fsw=6000;
Nsw=2*fsw/freq;
stepsw=1/fsw/2;
Tswo=2*stepsw;
Tswe=stepsw;
omegaL=omega*L;
a=Vpk/omegaL;
c=E0/L;
b=Ipk;
pflag=0;
nflag=0;
Bp(1)=1.6;
Bn(1)=-1.6;
pulse(1,1)=-1;

ierr=zeros(1,period*N);
ieave=zeros(2,period*fsw/freq);
Iref=zeros(1,period*N);
I=zeros(1,period*N);
pulse=zeros(1,period*N);
time=zeros(1,period*N);
clocko=zeros(1, period*Nsw);
clocke=zeros(1, period*Nsw);
```

```
zcpoint=zeros(1,period*N);
Tsp=zeros(1,period*N);
Tsn=zeros(1,period*N);
Tep=zeros(1,period*N);
Ten=zeros(1,period*N);
Bp=zeros(1,period*N);
Bn=zeros(1,period*N);

for i=1 : (period*N)
    time(1,i)=T;
    Iref(1,i)=Ipk*sin(omega*T);

    if i==1
        I(1,1)=-a*(cos(omega*T)-cos(omega*(T-step1)))-c*T*pulse(1,1);
    else
        I(1,i)=I(1,i-1)-a*(cos(omega*T)-cos(omega*(T-step1)))
               -c*step1*pulse(1,i);
    end;

    ierr(1,i)=I(1,i)-Iref(1,i);

    if i==1  zcpoint(1,1)=0;
             j=2;
    elseif   sign(ierr(1,i)*ierr(1,i-1))==-1
             zcpoint(1,j)=T;
             j=j+1;
             Vpk1=Vpk;
    end;

    if  mod(j,2)==0      k=j/2;
    end;

    if (j>2)&&(sign(ierr(1,i)*ierr(1,i-1))==-1)

        if      mod(j-1,2)==0
                Tsp(k)=zcpoint(1,j-1)-zcpoint(1,j-2);
                clocke(1,k)=Tswe;
                Tep(k)=zcpoint(j-1)-clocke(1,k);

Bp(k+1)=Bp(k)/Tsp(k)*(2*stepsw-Tep(k)+Bn(k)/Bp(k)*Tsp(k));
                Tswe=Tswe+2*stepsw;
```

```
            ieave(1,k)=zcpoint(1,j-1);
            ieave(2,k)=(Bp(k)+Bn(k))/2;
      elseif    mod(j-1,2)==1
            Tsn(k-1)=zcpoint(1,j-1)-zcpoint(1,j-2);
            clocko(1,k-1)=Tswo;
            Ten(k-1)=zcpoint(j-1)-clocko(k-1);

Bn(k)=Bn(k-1)/Tsn(k-1)*(2*stepsw-Ten(k-1)+Bp(k)/Bn(k-1)*Tsn(k-1));
            Tswo=Tswo+2*stepsw;
      end;

   end;

   if i<N*period

      if  (ierr(1,i)>Bp(k))&&(pflag==0)
            pulse(1,i+1)=1;
            pflag=1;
            nflag=0;
      elseif  (ierr(1,i)<Bn(k))&&(nflag==0)
            pulse(1,i+1)=-1;
            nflag=1;
            pflag=0;
      else
            pulse(1,1+i)=pulse(1,i);
      end;

   end;

   T=T+step1;

end;

figure (1);clf;
plot (time(:),ierr(:));
grid on;

figure (3); clf;
plot (time(:), Iref(:),'r');
hold on;
plot (time(1,:), I(:));
```

Appendix F

Relevant Mathematic Formulas

Trigonometric Functions and Relevant Identities

$$\sin^2\alpha+\cos^2\alpha=1 \tag{F.1}$$

$$\sin\alpha-\sin\beta=2\cos\frac{\alpha+\beta}{2}\sin\frac{\alpha-\beta}{2} \tag{F.2}$$

$$\cos\alpha-\cos\beta=-2\sin\frac{\alpha+\beta}{2}\sin\frac{\alpha-\beta}{2} \tag{F.3}$$

$$\cos(\alpha+\beta)=\cos\alpha\cos\beta-\sin\alpha\sin\beta \tag{F.4}$$

$$\sin(\alpha+\beta)=\sin\alpha\cos\beta+\cos\alpha\sin\beta \tag{F.5}$$

Taylor Expansion Theorem

$$f(x)=\sum_{n=0}^{m}(x-a)^n\cdot\frac{f^{(n)}(a)}{n!}+R_n(x) \tag{F.6}$$

Taylor Polynomials at zero for the sine and the cosine function

$$\sin x=x \tag{F.7}$$

$$\cos x=1-\frac{x^2}{2} \tag{F.8}$$